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A Study of the High Frequency Limitations of Series Resonant Converters

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Report

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NSG-3281

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by

Thomas A. Stuart

Roger J. King

Department of Electrical Engineering

University of Toledo

Toledo, Ohio 43606

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I. INTRODUCTION

This report presents the results of NASA Grant NSG-3281, "A Study of the High Frequency Limitations of Series Resonant Converters", for the period September 1981 to August 1982. This research was performed by the University of Toledo for the NASA Lewis Research Center.

The basic intent of this project was twofold. The first objective was to study a transformer induced oscillation in series resonant (SR) converters that can lead to the loss of cyclic stability. This characteristic had been observed earlier in the project and has also been reported by others [9.]. The second objective was a general investigation of a power MOSFET version of the SR converter which would be capable of operating at resonance frequencies above 100 kHz. The purpose of this second study was to identify some of the problems at these higher frequencies and to learn more about the upper frequency limitations. Both studies are now complete and are described in the following sections.

II. TRANSFORMER INDUCED INSTABILITY IN THE HALF BRIDGE CONVERTER

Because of its widespread usage throughout the aerospace industry, numerous papers have been presented on the characteristics of the series resonant (SR) power converter [1-12]. As a result, the advantages of this circuit are well known. It is presently capable of efficient operation at frequencies above 100 kHz with relatively minor stress on the active switching devices. This produces an inherently high power to weight ratio, making the circuit quite attractive for numerous applications.

Like all power conversion circuits however, the SR converter is subject to some potential problems, and careful design is required to achieve reliable operation. One of the more subtle difficulties is a transformer induced low frequency oscillation that may occur in the discontinuous current mode. The source of this oscillation is an unexpected resonant circuit formed by the normal LC resonance components in series with the magnetizing inductance of the output transformer. Once it occurs, it can lead to the loss of cyclic stability, making the circuit virtually inoperable at light loads. It should also be emphasized that the cause of this oscillation is not related to feedback, and it can occur in both open and closed loop circuits. The physical reasons for this problem and one possible solution have been reported previously in [9.], but to date no analytical model has been presented. Because of the numerous applications and the potential seriousness of this problem, a more detailed analysis seems appropriate.

The problem can be explained by referring to the half bridge circuit in Fig. 1 and the discontinuous mode waveforms in Fig. 2. Fig. 1(a.) shows the actual schematic while Fig. 1(b.) represents an equivalent circuit. Since the $R_L C_0$ product is assumed to be much larger than the switching time intervals, the load in Fig. 1(b.) is represented by an ideal voltage source V_0, reflected

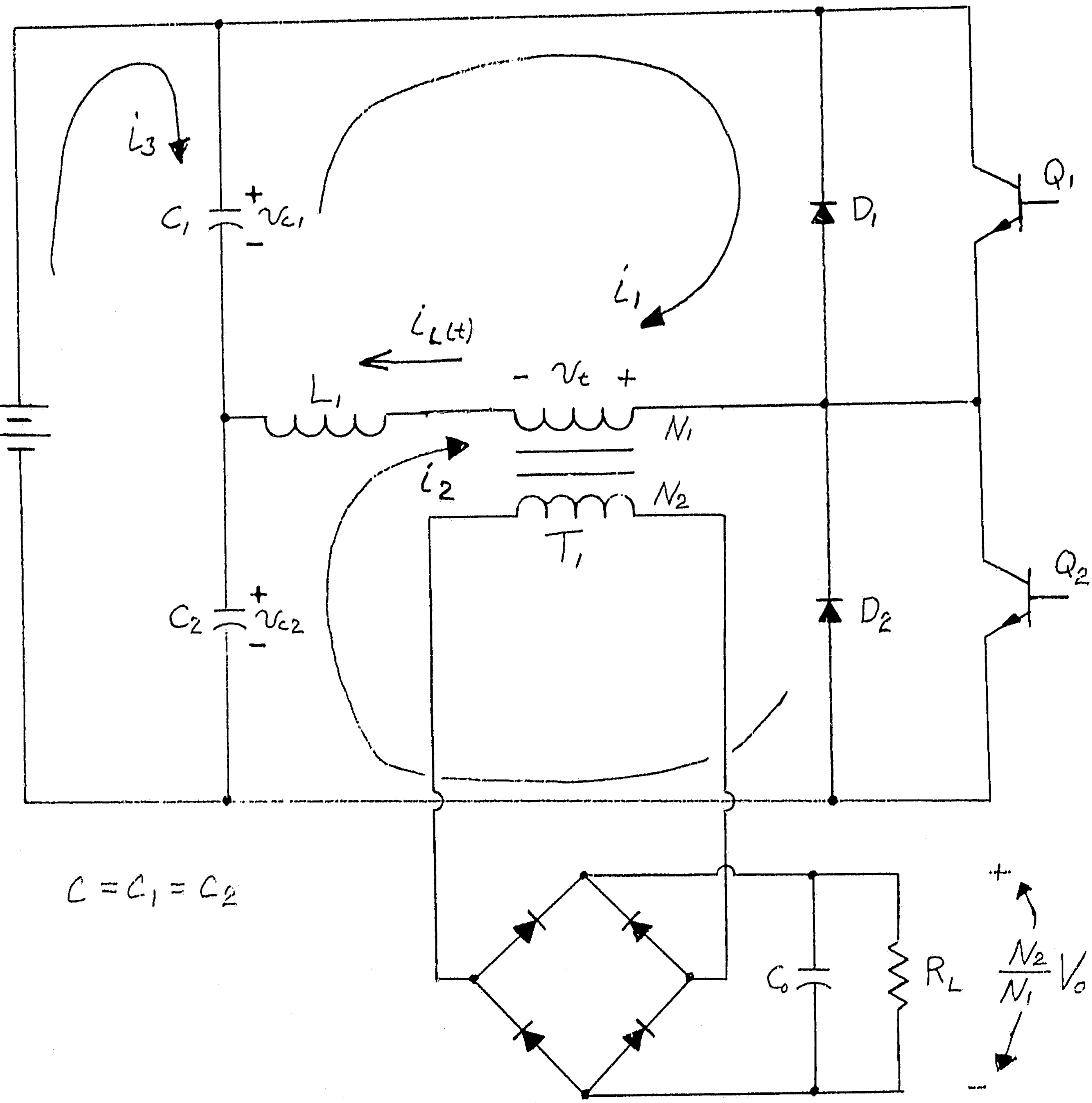
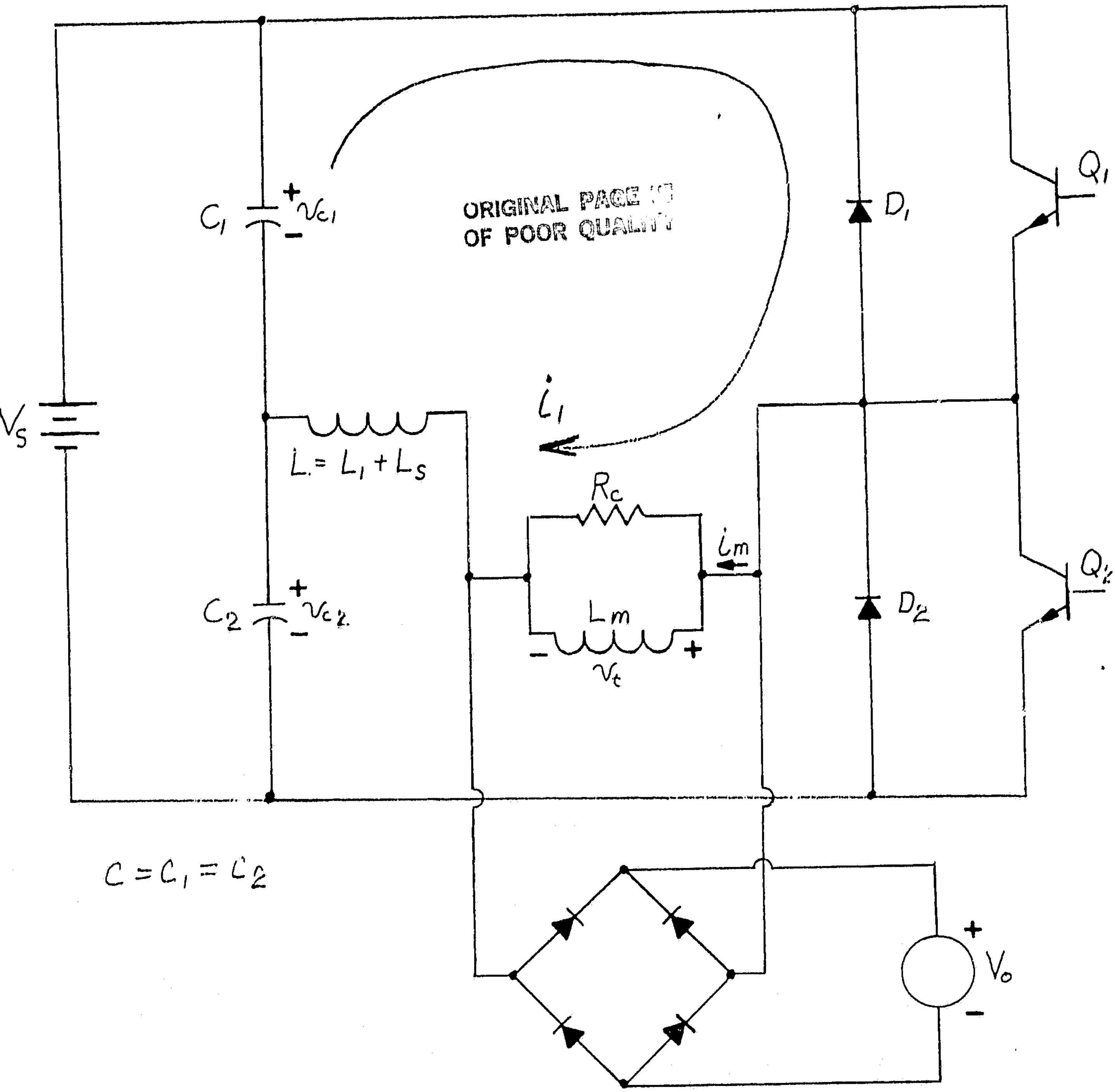


Fig. 1(a). Half Bridge Series Resonant Converter



L_s = Leakage Inductance

L_m = Magnetizing Inductance

R_c = Core Loss Resistance

Fig. 1(b). Half Bridge Equivalent Circuit

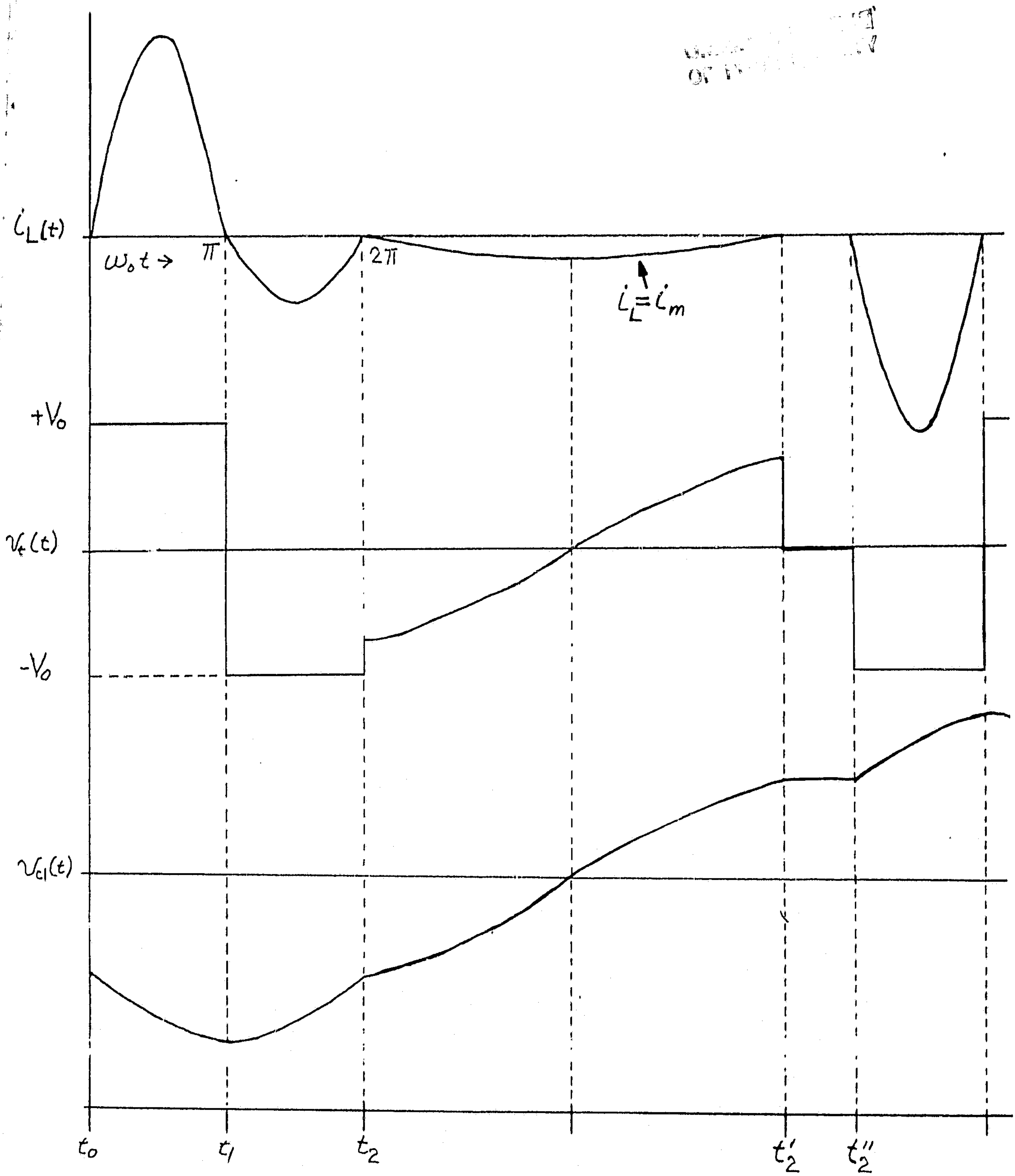


Fig. 2. Discontinuous Current Mode Waveforms

to the primary. Likewise the transformer is represented by the equivalent core loss resistance R_c, magnetizing inductance L_m and leakage inductance L_s (which is lumped with L_1). Otherwise, all components are assumed to be ideal. The desired operating sequence in the discontinuous mode is as follows: 1.) Q_1 fires and i_1 flows as indicated in Figs. 1 and 2, 2.) C_1 charges to a peak negative value, i_1 goes to zero and reverses through D_1 and then ceases at t_2, 3.) the sequence repeats for Q_2 and D_2 (note that the polarity of v_t will change to always oppose the primary current).

If the transformer were ideal ($L_m = \infty$, $R_c = \infty$), we would have ($i_1(t) = 0$ for the interval $t_2 \leq t \leq t_2'$ (the output rectifiers would be biased off during this interval since $|V_o| > |v_{c1}(t_2)|$). However since $v_{c1}(t_2) < 0$, current can flow through R_c and L_m during $t_2 \leq t \leq t_2'$ as indicated in Fig. 2. Thus the voltage across C_1 can reverse, producing a $v_{c1}(t_2') > 0$, and if Q1 is blocking, it will remain at this value until the next half cycle starts at t_2'', i.e., $v_{c1}(t_2') = v_{c1}(t_2'')$. Now $v_{c2}(t_2'') = V_s - v_{c1}(t_2'')$, and if $v_{c2}(t_2'') < |V_o|$ the next half cycle will not start. This implies that the circuit no longer has cyclic stability.

Based on the above analysis, we can state the following necessary condition for cyclic stability in the discontinuous mode:

$$V_s - v_{c1}(t_2') > |V_o|. \qquad (1.)$$

There are at least three basic methods of achieving the condition defined by (1.) and these will be treated in detail in the following sections.

The analysis presented here builds on an earlier steady state model originally derived in [1.]. This previous model is adequate for most steady state calculations, but it assumes an ideal transformer (i.e., $R_c = \infty$, $L_m = \infty$), and thus ignores the possibility of any transformer related oscillations.

The model from [1.] can be readily extended to include these transformer effects however, and the methods for achieving the stability condition of (1.) will be discussed.

NOMENCLATURE

A, B	=	Terms defined by (35.)
$C = C_1 = C_2$	=	Capacitance value of resonance capacitors
C_o	=	Output filter capacitor
E_L	=	Energy supplied to load
E_S	=	Energy obtained from source
I_{avg}	=	Half cycle average output current at primary of transformer
$I_{D\ avg}$	=	Average diode current
I_{LO}	=	i_L @ $t = 0$
I_{peak}	=	Peak value of output current at primary of transformer
$I_{Q\ avg}$	=	Average transistor current
I_{RMS}	=	RMS output current at primary of transformer
$i_{1,2,3}$	=	Loop currents
$i_L = i_1 - i_2$	=	Output current at primary of transformer
L_m	=	Transformer magnetizing inductance
L_s	=	Transformer leakage inductance
L_1	=	Inductance value of resonance inductor
L	=	$L_1 + L_s$
q	=	Normalized load voltage defined by (2) (also see (29.))
q'	-	Value of q when D_1 or D_2 conducts (also see (29.))

R_c	=	Equivalent core loss resistance
R_{ext}	=	External resistor
R_L	=	Load resistor
$V_{c\ peak}$	=	Peak capacitor voltage
V_{ci}	=	Voltage across capacitor C_i
V_{ij}	=	Voltage across capacitor i at time t_j
V_0	=	Amplitude of square-wave output voltage at primary of transformer. V_0 is always considered positive.
V_s	=	DC source voltage
v_t	=	Instantaneous primary voltage
Z_m	=	Impedance term defined by (6.)
Z_o	=	Impedance defined above (20.) (also see (29))
α	=	Delay angle
β	=	Transistor conduction angle
ψ	=	Reduction factor defined by (11.)
ω_m	=	Resonance frequency defined by (6.)
ω_o	=	Resonance frequency defined above (20.) (also see (29.))

<u>Half Bridge Model with Transformer Effects</u>:

Consider the circuit at $t = t_2$ (see Fig. 2). We see that if $v_{c1}(t_2) \geq 0$, no low frequency oscillation from t_2 to t_2' will occur since Q_1 is turned off prior to t_2. From [1.],

$$v_{c1}(t_2) \equiv V_{12} = \frac{V_s}{2}(1 - 2q) \tag{2.}$$

$$\text{where } q \equiv \frac{2V_o}{V_s}, \quad (0 \leq q < 1)$$

$$\therefore V_{12} \geq 0 \Rightarrow q \leq .5 \tag{3.}$$

This implies that the circuit will behave as predicted by the ideal model of [1.], and cyclic stability is preserved. Therefore we can state,

Rule H-1: The half bridge, SR converter will avoid transformer induced instability in the discontinuous mode if $q \leq 0.5$.

Unfortunately, Rule H-1 does not provide a very practical means for achieving stability. To fully utilize the power handling capability of the circuit, q should be as close to 1.0 as possible. By the same reasoning as used above, we see that the low frequency oscillation may occur if $V_{12} < 0$, or from (2.),

$$V_{12} < 0 \Rightarrow q > .5 \tag{4.}$$

In this case, if R_c is ignored,

$$i_1(t') = \frac{V_{12}}{Z_m} \sin\omega_m t' \quad , \quad 0 \leq t' \leq t_2'-t_2 \tag{5.}$$

where,
$$Z_m = \sqrt{\frac{L+L_m}{2C}} \quad , \quad \omega_m = \frac{1}{\sqrt{2C(L+L_m)}} \tag{6.}$$

and
$$\omega_m(t_2' - t_2) = \pi \tag{7.}$$

From [1.], $i_3(t) = \dfrac{i_1(t)}{2}$, and therefore

$$v_{c1}(t') = V_{12} - \int_0^{t'} \frac{1}{2C} \cdot \frac{V_{12}}{Z_m} \sin\omega_m t' dt' \tag{8.}$$

$$\therefore v_{c1}(t') = V_{12}\cos\omega_m t' \quad , \quad 0 \leq t' \leq t_2' - t_2 \tag{9.}$$

and
$$v_{c1}(t_2') \equiv V_{12'} = -V_{12} \tag{10.}$$

Now suppose we include the effect of the core loss resistance R_c in Fig. 1. However, instead of using the exact equations we merely observe that $|V_{12'}|<|V_{12}|$ because of the R_c losses. Therefore,

$$V_{12'} = -\psi \, V_{12} \tag{11.}$$

where $0 \leq \psi \leq 1$ is defined to be the reduction factor. (Note that R_c will not affect the calculations for $0 \leq t \leq t_2$ since it is in parallel with the load during this time). Cyclic stability implies that $v_{c1}(t_2') = v_{c2}(t_o)$, or equivalently,

$$V_s - V_{10} = V_{12'} = -\psi \, V_{12} \tag{12.}$$

where $\quad V_{10} \equiv v_{c1}(t_o)$

From [1.], we have,

$$V_{12} = V_{10} - 4V_o \tag{13.}$$

$$\therefore \; V_s - V_{10} = -\psi \, (V_{10} - 4V_o) \tag{14.}$$

and

$$V_{10} = 2V_o \frac{\left(\frac{1}{q} - 2\psi\right)}{(1-\psi)} \tag{15.}$$

For the Q_1 half cycle to take place, we must have $V_{10} > V_o$. Therefore,

$$\psi < \frac{2}{3q} - \frac{1}{3} \tag{16.}$$

A plot of the stable ψ vs. q region is shown in Fig. 3. Observe that ψ must be lower for higher values of q, i.e., an external resistance, R_{ext},

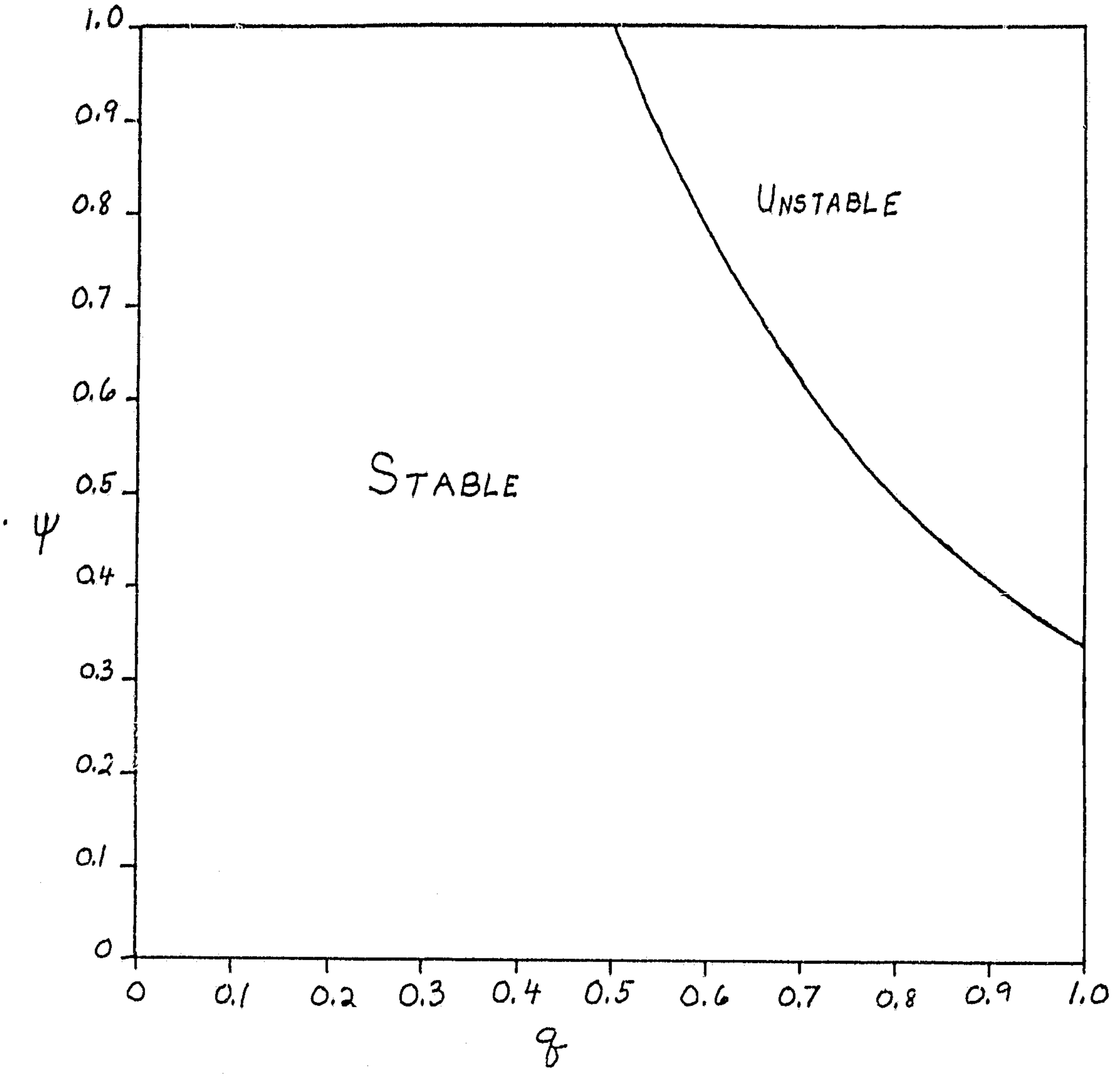


Fig. 3. Stable and Unstable ψ vs. q Regions for the Half Bridge SR Converter.

must be placed in parallel with R_c to provide more damping. Although R_{ext} would have to be found experimentally, this does indicate a second way to avoid the transformer instability, and we state,

Rule H-2: For .5 < q < 1.0, the half bridge SR converter will avoid transformer induced instability in the discontinuous mode if $\psi < \frac{2}{3q} - \frac{1}{3}$ (however, the low frequency oscillation may still be present).

Although there is a loss in efficiency, Rule H-2 indicates a simple means of eliminating the instability. In practice, R_{ext} should not be placed directly in parallel with the transformer primary but rather as indicated in Fig. 4. Here for example, during the Q1-D1 conduction interval the auxilliary diode D_3 conducts only while v_t in Fig. 2 is negative. This greatly reduces the losses in R_{ext}, especially under high load voltage, continuous current operation. The proper value of R_{ext} is about the same for either connection.

It should be noted that this ψ factor will alter the steady state equations of [1.] for the discontinuous mode. However, several of these variables are functions of V_{10} and/or V_{11} ($V_{11} \equiv v_{c1}(t_1)$), and these can be readily determined. From (15.),

$$V_{10} = V_s \left(\frac{1-2\ \psi q}{1-\psi}\right) \tag{17.}$$

From [1.],

$$V_{11} = 2V_o - V_{10} \tag{18.}$$

$$\therefore V_{11} = V_s \left(\frac{q-1+q\psi}{1-\psi}\right) \tag{19.}$$

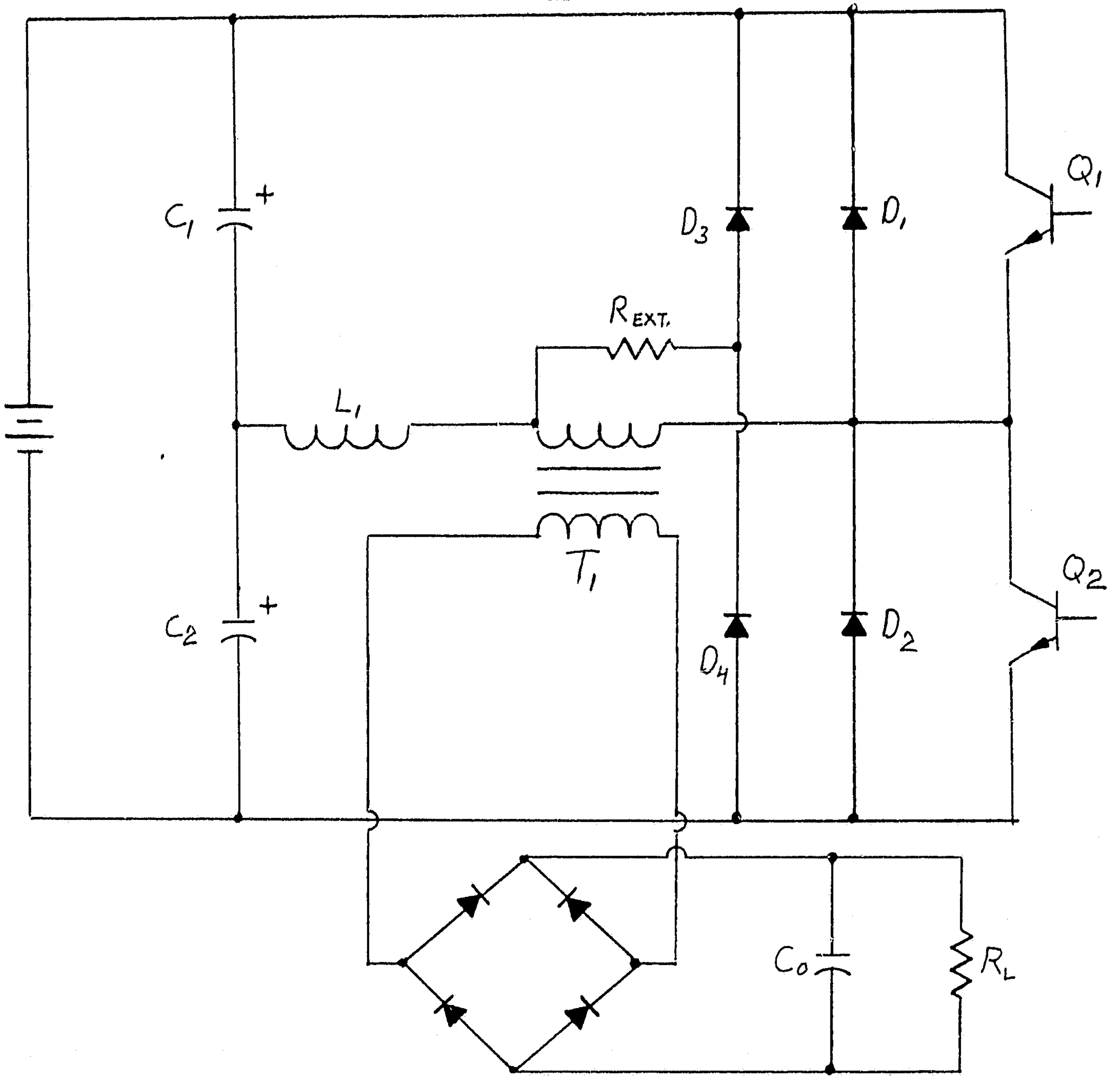


Fig. 4. Preferred Connection of Parallel Damping Resistance. Diodes D_3 or D_4 only Conduct When D_1 or D_2 Conduct.

Setting $\psi = -1$ in (17.) and (19.) produces the same V_{10} and V_{11} as in [1.] (i.e., this would correspond to the case where no low frequency oscillation occurred and $V_{12''} = V_{12}$).

From [1.], we have the following equations for $i_1(t)$ in the discontinuous mode, ($Z_o = \sqrt{L/2C}$, $\omega_o = 1/\sqrt{2LC}$),

$$i_1(t) = \frac{V_{10}-V_o}{Z_o} \sin(\omega_o t) \quad , \quad 0 \le t \le t_1 \tag{20.}$$

$$i_1(t') = \frac{V_{11}+V_o}{Z_o} \sin(\omega_o t') \quad , \quad 0 \le t' \le t_2-t_1 \tag{21.}$$

$$\therefore I_Q \text{ avg} = \frac{1}{2(\pi+\alpha)} \int_0^{\pi} \frac{V_{10}-V_o}{Z_o} \sin(\omega_o t)\, d\omega_o t = \frac{(V_{10}-V_o)}{Z_o(\pi+\alpha)} \tag{22.}$$

$$\text{and, } I_{peak} = \frac{V_{10}-V_o}{Z_o} \tag{23.}$$

If we ignore the low frequency current during $t_2 \le t \le t_2'$,

$$I_{D\ avg} \doteq \frac{-1}{2(\pi+\alpha)} \int_0^{\pi} \frac{V_{11}+V_o}{Z_o} \sin(\omega_o t')\, d\omega_o t' = \frac{-(V_{11}+V_o)}{Z_o(\pi+\alpha)} \tag{24.}$$

And the approximate average half cycle load current on the primary would be,

$$I_{avg} \doteq 2\left(I_{Q\ avg} + I_{D\ avg}\right) = \frac{2(V_{10}-V_{11}-2V_o)}{Z_o(\pi+\alpha)} \tag{25.}$$

Finally, we have the approximate RMS primary load current,

$$I_{rms} \doteq \left\{ \frac{1}{\pi+\alpha} \left[\int_{o}^{\pi} \left(\frac{V_{10}-V_o}{Z_o} \right)^2 \sin^2(\omega_o t)\, d\omega_o t \right. \right.$$

$$\left. \left. + \int_{o}^{\pi} \left(\frac{V_{11}+V_o}{Z_o} \right)^2 \sin^2(\omega_o t')\, d\omega_o t' \right] \right\}^{1/2}$$

$$= \frac{1}{Z_o} \left\{ \frac{\pi}{2(\pi+\alpha)} \left[\left(V_{10}-V_o\right)^2 + \left(V_{11}+V_o\right)^2 \right] \right\}^{1/2} \qquad (26.)$$

To find the peak capacitor voltage, we note that the peak negative voltage across C_1 will occur at t_1 where $i_1(t)$ reverses. This corresponds to the peak positive voltage across C_2 since,

$$V_{Cpeak} = v_{c2}(t_1) \equiv V_{21} = V_s - V_{11} \qquad (V_{11} \text{ is negative}) \qquad (27.)$$

A third method for avoiding the transformer instability problem is to change the value of the reflected load voltage during the D_1 and D_2 conduction intervals. This implies that the magnitude of v_t must be altered during these periods. There are probably several ways of implementing this, one being the method used in [9.] which is shown in Fig. 5.

The intent of this circuit is to have Q_3 conduct for certain discontinuous modes whenever D_1 or D_2 conducts. This sets $v_t = 0$ during these periods and thus creates a new $q' = 0$ (although we define $q = 2\, V_o/V_s$, on an instantaneous basis we actually have $q = 2\, v_t/V_s$). Fig. 5 probably represents the most practical implementation of this approach, but it is not absolutely necessary that the new $q' = 0$. Therefore for the sake of generality,

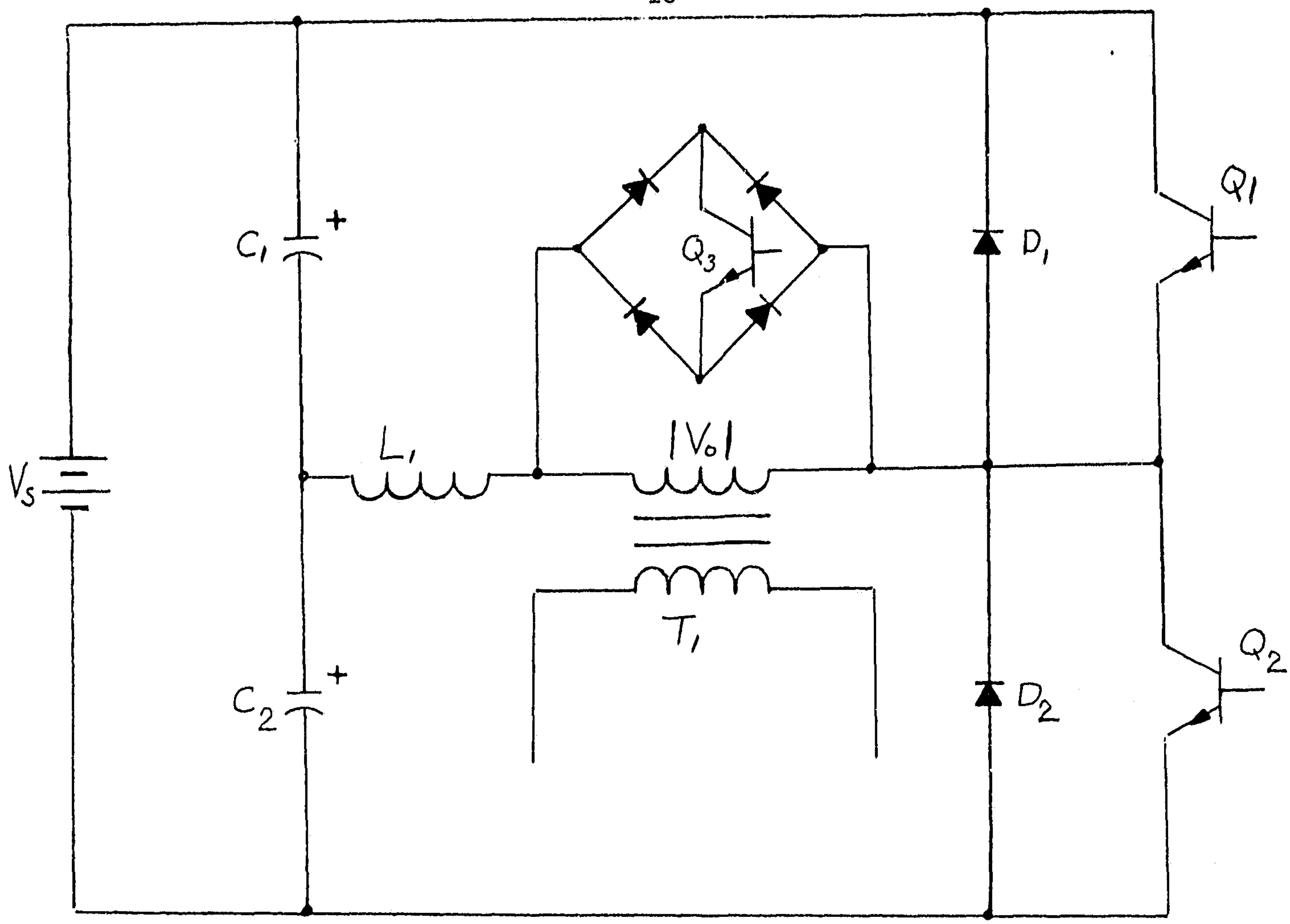


Fig. 5. Circuit for Creating a New $q'=0$ During the D_1 and D_2 Conduction Intervals

the value of q' (which applies for the diode conduction interval) will not be restricted to zero in the new model. One possible method of implementing a circuit that would switch from a value of q to a non-zero value of q' would be to connect D_1 and D_2 to a tap on the primary instead of to the emitter of Q_1. The characteristics of such an arrangement were not investigated however.

Ideally, one would prefer to create this new q' only during the discontinuous mode. However, in some cases it may be difficult to implement this exactly and the new q' also may apply during continuous operation as the discontinuous mode is approached. Therefore, the new model will assume a normalized load voltage, q, whenever Q_1 or Q_2 conduct and a normalized load voltage, q', whenever D_1 or D_2 conduct in both the continuous and discontinuous modes. For those continuous modes where q does not change, the original model derived in [1.] still applies.

Proceeding as in [1.], we define the following terms, ($C = C_1 = C_2$)

$$V_{10} \equiv v_{c1}(0), \quad V_{11} \equiv v_{c1}(t_1), \quad V_{12} \equiv v_{c1}(t_2)$$

$$V_{20} \equiv v_{c2}(0) = V_s - V_{10}, \quad V_{21} \equiv v_{c2}(t_1) = v_s - V_{11} \tag{28.}$$

$$\omega_o \equiv \frac{1}{\sqrt{2LC}}, \quad Z_o \equiv \sqrt{L/2C}, \quad q \equiv \frac{2V_o}{V_s}, \quad q' \equiv \frac{2V'_o}{V_s} \tag{29.}$$

(i.e., $|v_t| = V_o$ for $0 \leq t \leq t_1$, $|v_t| = V'_o$ for $t_1 \leq t \leq t'_2$).

$\alpha = \omega_o\,(t_2 - t_1)$ where $\alpha \leq 180°$ for continuous conduction,

$$\beta \equiv \omega_o t_1, \quad t' = t - t_1 \tag{30.}$$

If Q_1 is turned on at $t = 0$ and Q_2 at t_2, we have for the continuous case,

$$i_1(0) \equiv I_{LO}$$

$$i_1(t) = I_{LO}\cos\omega_o t + \frac{V_{10}-V_0}{Z_o}\sin\omega_o t \quad , \quad 0 \leq t \leq t_1 \tag{31.}$$

$$i_1(t') = \frac{V_{11}+V'_0}{Z_o}\sin\omega_o t' \quad , \quad 0 \leq t' \leq t_2-t_1 \tag{32.}$$

$$v_{c1}(t) = -I_{LO}Z_o\sin\omega_o t + (V_{10}-V_0)\cos\omega_o t + V_0 \quad , \quad 0 \leq t \leq t_1 \tag{33.}$$

$$v_{c1}(t') = (V_{11} + V'_0)\cos\omega_o t' - V'_0 \quad , \quad 0 \leq t' \leq t_2 - t_1 \tag{34.}$$

Define the quantities A and B,

$$A \equiv \omega_o \int_o^{t_1} i_1(t)dt \quad , \quad B \equiv -\omega_o \int_0^{t_2-t_1} i_1(t')dt' \tag{35.}$$

Therefore,

$$A = I_{LO}\sin\beta + \frac{(V_{10}-V_0)}{Z_o}(1-\cos\beta) \tag{36.}$$

$$B = \frac{(V_{11}+V'_0)}{Z_o}(\cos\alpha - 1) \tag{37.}$$

Now,

$$V_{11} = v_{c1}(t_1) = -I_{LO}Z_o\sin\beta + (V_{10}-V_0)\cos\beta + V_0 \tag{38.}$$

$$\therefore B = (1-\cos\alpha)\left(A - \frac{V_{10}+V'_0}{Z_o}\right) \tag{39.}$$

From (36.) and (38.),

$$V_{11} = -A\ Z_o + V_{10} \tag{40.}$$

From (34.) with $\alpha = \omega_o(t_2 - t_1)$,

$$V_{12} = (V_{11} + V_o') \cos\alpha - V_o' \tag{41.}$$

And from (39.) , (40.) and (41.),

$$V_{12} = B\ Z_o - A\ Z_o + V_{10} \tag{42.}$$

For cyclic stability,

$$V_s - V_{10} = V_{12} = B\ Z_o - A\ Z_o + V_{10} \tag{43.}$$

$$V_{10} = \frac{V_s + (A-B)\ Z_o}{2} \tag{44.}$$

From (40.),

$$V_{11} = \frac{V_s - (A+B)\ Z_o}{2} \tag{45.}$$

and from (42.),

$$V_{12} = \frac{V_s - (A-B)\ Z_o}{2} \tag{46.}$$

The energy into the load during $0 \leq t \leq t_2$ is,

$$E_L = |V_o| \int_0^{t_1} i_1(t)\,dt - |V_o'| \int_0^{t_2-t_1} i_1(t')\,dt'$$

$$= \frac{|V_o| A}{\omega_o} + \frac{|V_o'| B}{\omega_o} \tag{47.}$$

Since $i_3 = i_1/2$ for $0 \leq t \leq t_2$, the energy from V_s during this period is,

$$E_s = V_s \int_0^{t_1} \frac{i_1(t)}{2}\, dt + V_s \int_0^{t_2-t_1} \frac{i_1(t')}{2}\, dt'$$

$$= \frac{V_s A}{2\omega_o} - \frac{V_s B}{2\omega_o} \qquad (48.)$$

It can be shown that the stored energy at t_2 is the same as at t_0. Therefore,

$$E_s = E_L \qquad (49.)$$

or from (47.) and (48.),

$$B = A\left(\frac{1-q}{1+q'}\right) \qquad (50.)$$

from (39.) and (50.),

$$A\left(\frac{1+q}{1+q'}\right) = (1-\cos\alpha)\left(A - \frac{V_{10} + V_0'}{Z_o}\right) \qquad (51.)$$

and from (44.)

$$A\left[\frac{1-q}{1+q'} - (1-\cos\alpha)\right] = (1-\cos\alpha)\left[-\frac{V_s}{2Z_o} - \frac{(A-B)}{2} - \frac{V_o'}{Z_o}\right] \qquad (52.)$$

$$A = \frac{V_s}{2Z_o}\left[\frac{2(1+q')^2\,(1-\cos\alpha)}{q+q' - (2+q'-q)\cos\alpha}\right] \qquad (53.)$$

$$B = \frac{V_s}{2Z_o}\left[\frac{2(1-q)\,(1+q')\,(1-\cos\alpha)}{q+q' - (2+q'-q)\cos\alpha}\right] \qquad (54.)$$

Now,

$$A - B = A\left(\frac{q+q'}{1+q'}\right) \quad , \quad A + B = A\left(\frac{2+q'-q}{1+q'}\right) \tag{55.}$$

Therefore from (44.) - (46.),

$$V_{10} = \frac{V_s}{2}\left[1 + \frac{(q+q')\ (1+q')\ (1-\cos\alpha)}{(q+q') - (2+q'-q)\ \cos\alpha}\right] \tag{56.}$$

$$V_{11} = \frac{V_s}{2}\left[1 - \frac{(2+q'-q)\ (1+q')\ (1-\cos\alpha)}{(q+q') - (2+q'-q)\ \cos\alpha}\right] \tag{57.}$$

$$V_{12} = \frac{V_s}{2}\left[1 - \frac{(q+q')\ (1+q')\ (1-\cos\alpha)}{(q+q') - (2+q' - q)\ \cos\alpha}\right] \tag{58.}$$

and from (27.),

$$V_{c\ peak} = \frac{V_s}{2}\left[1 + \frac{(2+q'-q)\ (1+q')\ (1-\cos\alpha)}{(q+q') - (2+q'-q)\ \cos\alpha}\right] \tag{59.}$$

For cyclic stability, note from (32.) that,

$$-I_{LO} = \frac{V_{11} + V'_o}{Z_o} \sin\alpha \tag{60.}$$

Therefore from (53.), (55.) and (57.),

$$I_{LO} = \frac{V_s}{2Z_o}\left[\frac{2(1-q)\ (1+q')\ \sin\alpha}{(q+q') - (2+q'-q)\ \cos\alpha}\right] \tag{61.}$$

To find the angle β, note from (31.),

$$\tan\beta = \frac{-I_{L0}Z_0}{V_{10}-V_0} \tag{62.}$$

Therefore from (56.) and (61.),

$$\beta = \tan^{-1}\left\{\frac{-2(1-q)\ (1+q')\sin\alpha}{(q+q')\ (2+q'-q)\ -\left[(1+q')^2 + (1-q)^2\right]\cos\alpha}\right\} + \pi \quad (63.)$$

The average rectified value of $i_1(t)$ is,

$$I_{avg} = \frac{1}{t_2}\left[\int_0^{t_1} i_1(t)\,dt - \int_0^{t_2-t_1} i_1(t')\,dt'\right] \quad (64.)$$

or from (35.),

$$I_{avg} = \frac{A+B}{\alpha+\beta} \quad (65.)$$

and from (53.) and (55.),

$$I_{avg} = \frac{V_s}{2Z_o}\left\{\frac{2(1+q')\ (2+q'-q)\ (1-\cos\alpha)}{\left[(q+q')\ -\ (2+q'-q)\ \cos\alpha\right]\ (\alpha+\beta)}\right\} \quad (66.)$$

In a similar manner we can find the average transistor current and the average diode current,

$$I_{Q\ avg} = \frac{A}{2(\alpha+\beta)} = \frac{V_s}{2Z_o}\left\{\frac{(1+q')^2\ (1-\cos\alpha)}{\left[(q+q')\ -\ (2+q'-q)\ \cos\alpha\right]\ (\alpha+\beta)}\right\} \quad (67.)$$

$$I_{D\ avg} = \frac{B}{2(\alpha+\beta)} = \frac{V_s}{2Z_o}\left\{\frac{(1-q)\ (1+q')\ (1-\cos\alpha)}{\left[(q+q')\ -\ (2+q'-q)\ \cos\alpha\right]\ (\alpha+\beta)}\right\} \quad (68.)$$

For the RMS current we have,

$$I_{RMS} = \left\{\frac{1}{t_2}\left[\int_0^{t_1}\left(I_{Lo}\cos\omega_o t + \frac{V_{10}-V_o}{Z_o}\sin\omega_o t\right)^2 dt + \int_0^{t_2-t_1}\left(\frac{V_{11}+V_o'}{Z_o}\sin\omega_o t'\right)^2 dt'\right]\right\}^{1/2} \quad (69.)$$

$$\therefore\ I_{RMS} = \left\{ \frac{1}{\alpha+\beta} \left[I_{LO}^2 \left(\frac{\beta}{2} + \frac{\sin 2\beta}{4} \right) + \left(\frac{V_{10}-V_0}{Z_o} \right)^2 \left(\frac{\beta}{2} - \frac{\sin 2\beta}{4} \right) \right.\right.$$

$$\left.\left. + \frac{I_{LO}\,(V_{10}-V_0)}{Z_o} \sin^2\beta + \left(\frac{V_{11}+V'_o}{Z_o} \right)^2 \left(\frac{\alpha}{2} - \frac{\sin 2\alpha}{4} \right) \right] \right\}^{1/2} \qquad (70.)$$

As in [1.], it can be shown that the peak value of $i_1(t)$ is,

$$I_{peak} = I_{LO} \sin\beta - \frac{V_{10}-V_0}{Z_o} \cos\beta \qquad (71.)$$

Comparing (36.) and (71.),

$$I_{peak} = A - \frac{V_{10}-V_0}{Z_o} \qquad (72.)$$

From (53.) and (56.),

$$I_{peak} = \frac{V_s}{2Z_o} \left\{ \frac{(1+q')^2 + (1-q)^2 + [(1-q)^2 - (1+q')^2] \cos\alpha}{(q+q') - (2+q'-q) \cos\alpha} \right\} \qquad (73.)$$

The discontinuous current expressions may be found by setting $\beta = \pi$ everywhere, and $\alpha = \pi$ everywhere except where α represents the averaging period. Therefore from (56.)-(59.), (66.)-(68.), (70.) and (73.),

$$V_{10} = \frac{V_s}{2} \ (1+q+q') \qquad (74.)$$

$$V_{11} = \frac{V_s}{2} \ (-1+q-q') \qquad (75.)$$

$$V_{12} = \frac{V_s}{2} \ (1-q-q') \qquad (76.)$$

$$V_{C\ peak} = \frac{V_s}{2} \ (3-q+q') \tag{77.}$$

$$I_{L0} = 0 \tag{78.}$$

$$I_{avg} = \frac{V_s}{2Z_o}\left[\frac{2(2+q'-q)}{\pi+\alpha}\right] \tag{79.}$$

$$I_{Q\ avg} = \frac{V_s}{2Z_o}\left(\frac{1+q'}{\pi+\alpha}\right) \tag{80.}$$

$$I_{D\ avg} = \frac{V_s}{2Z_o}\left(\frac{1-q}{\pi+\alpha}\right) \tag{81.}$$

$$I_{RMS} = \frac{1}{Z_o}\left\{\frac{\pi}{2(\pi+\alpha)}\left[(V_{10}-V_0)^2 + (V_{11}+V_o')^2\right]\right\}^{1/2} \tag{82.}$$

$$I_{peak} = \frac{V_s}{2Z_o} \ (1+q') \tag{83.}$$

This completes the derivation of the steady state equations for a circuit with different values for q and q'. We now consider the restrictions on q and q' that are necessary for cyclic stability in the discontinuous mode. For the previously described low frequency oscillation to occur, it is necessary that,

$$V_{12} = \frac{V_s}{2} \ (1-q-q') < 0 \tag{84.}$$

$$\text{or } (q+q') > 1 \tag{85.}$$

If the oscillation does occur and R_C [illegible],

$$V_{12'} = -V_{12} \tag{86.}$$

Cyclic stability requires that $V_{12'} = V_{20}$ or,

$$V_s - V_{10} = V_{12'} = -V_{12} \tag{87.}$$

From (38.) we have for the discontinuous mode

$$V_{11} = 2V_o - V_{10} \tag{88.}$$

From (41.) we have

$$V_{12} = -V_{11} - 2V_o' = V_{10} - 2V_o - 2V_o'. \tag{89.}$$

Therefore, for cyclic stability we require

$$V_s - V_{10} = -(V_{10} - 2V_o - 2V_o') \tag{90.}$$

which shows that the solution for V_{10} is indeterminate. This indicates that the necessary V_{10} for cyclic stability with $R_c = \infty$ cannot be found, i.e., it does not exist if $(q+q') > 1$. Therefore the circuit must be constrained so that the low frequency oscillation does not occur, meaning $(q+q') < 1$. We can now state,

Rule H-3: For the half bridge SR converter with normalized load voltage q for $0 \leq t \leq t_1$, and q' for $t_1 < t \leq t_2'$, transformer induced instability in the discontinuous mode will be avoided if $(q+q') < 1$.

Since $q < 1$, setting $q' = 0$ by shorting the transformer primary whenever D_1 or D_2 conducts will insure cyclic stability for all acceptable values of q. Strictly speaking however, q' can have any value over the range $0 \leq q' < 1 - q$. Although its implementation is more complex, Rule H-3 probably indicates the most efficient solution to the stability problem. Values of q close to 1.0 can be used, and no lossy damping components are required.

Experimental Results

The nature of the transformer induced oscillation is illustrated by comparison of Figs. 6 and 7. These waveforms were obtained from a conventional 150 watt SR converter operating at a natural resonance frequency of 10 kHz. Fig. 6 shows v_{cl} and v_t under normal operating conditions with $q < 0.5$. This result is in agreement with Rule H-1, which states that the low frequency oscillation cannot occur if $q < 0.5$. Fig. 7 shows an oscillation on the same waveforms for the case where q is slightly greater than 0.5. The nature of the oscillation is perhaps most evident on the v_t trace. Immediately after the first negative half cycle of v_t, an oscillation of about 1.3 kHz occurs. It was possible to sustain the oscillation in this form only for values of q very close to 0.5. For larger q values, the oscillation leads to a loss of cyclic stability which produces totally erratic waveforms.

Rule H-2 states that transformer stability can also be achieved if a sufficiently small damping resistor, R_{ext}, is connected across the primary. This was also verified experimentally on the same 10 kHz, 150 watt circuit. This solution is probably less efficient than the other alternatives, but it is relatively simple and thus may be more reliable.

Rule H-3 states that transformer stability will be achieved if $q + q' < 1$, where q applies for $0 \leq t \leq t_1$ and q' applies for $t_1 < t \leq t_2'$. This arrangement was not tested in these experiments, since an implementation of this rule was reported earlier in [9.]. In this converter, the primary was shorted by a clamp circuit during the interval, $t_1 < t \leq t_2'$. This implies $q' = 0$, and therefore $q + q' < 1$ since $0 < q < 1$.

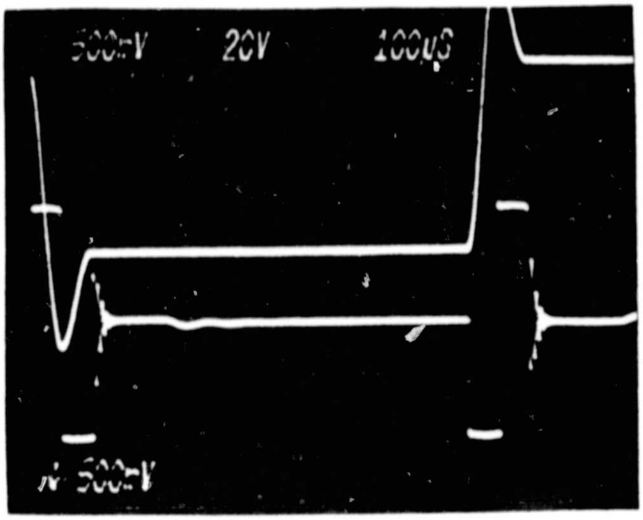


Fig. 6. Stable Operation with q < 0.5 (100us./div.)
Top: Capacitor Voltage, v_{c1}, vs. time
(50V./div.)
Bottom: Transformer Voltage, v_t, vs. time
(20V./div.)

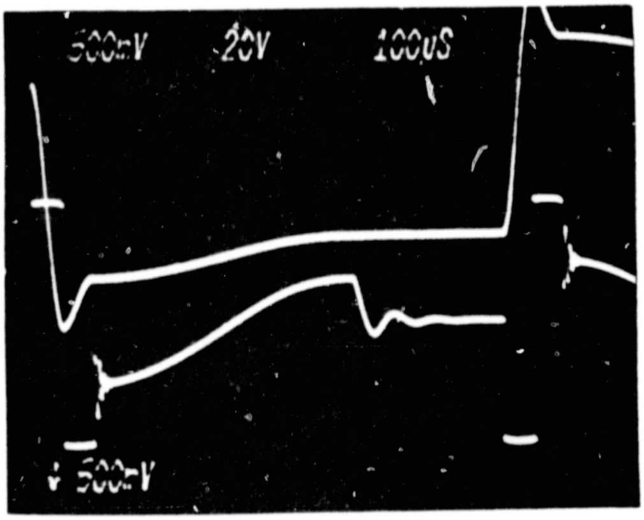


Fig. 7. Low Frequency Oscillation with q > 0.5 (100us./div.)
Top: Capacitor Voltage, v_{c1}, vs. time
(50V./div.)
Bottom: Transformer Voltage, v_t, vs. time
(20V./div.)

III. TRANSFORMER INDUCED INSTABILITY IN THE FULL BRIDGE CONVERTER

The analysis for the full bridge converter proceeds in much the same manner as that for the half bridge version. Using the previous transformer and load models, the equivalent full bridge circuit is shown in Fig. 8. The conduction sequence in this circuit is Q_1-Q_3, D_1-D_3, Q_2-Q_4, D_2-D_4. Referring to Fig. 8 and the i_L and v_t waveforms from Fig. 2 (i_L and v_t are the same for both the half and full bridge versions), we consider the discontinuous half cycle where Q_1 and Q_3 conduct from 0 to t_1 and D_1 and D_3 conduct from t_1 and t_2. At t_2, $v_c(t_2) < 0$. We see that if $V_s \geq -v_c(t_2)$, the low frequency oscillation from t_2 to t_2' will not occur since D_1 and D_3 will be reverse biased, and Q_1 and Q_3 have been turned off prior to t_2. From [12.],

$$v_c(t_2) = V_{c2} = V_s \left[\frac{q(1+q)(1-\cos\pi)}{q-\cos\pi}\right]$$

$$\text{or} \quad V_{c2} = -2qV_s \tag{1.}$$

$$\therefore V_s + V_{c2} = V_s(1-2q) \geq 0 \Rightarrow q \leq 0.5 \tag{2.}$$

Thus Rule H.1, derived in the previous section for the half bridge circuit, also applies for the full bridge converter. Therefore we can state,

<u>Rule F.1</u>: Same as Rule H.1.

Conversely, the low frequency oscillation can occur if $V_s + V_{c2} < 0$, or from (2.),

$$V_s + V_{c2} = V_s(1-2q) < 0 \Rightarrow q > .5 \tag{3.}$$

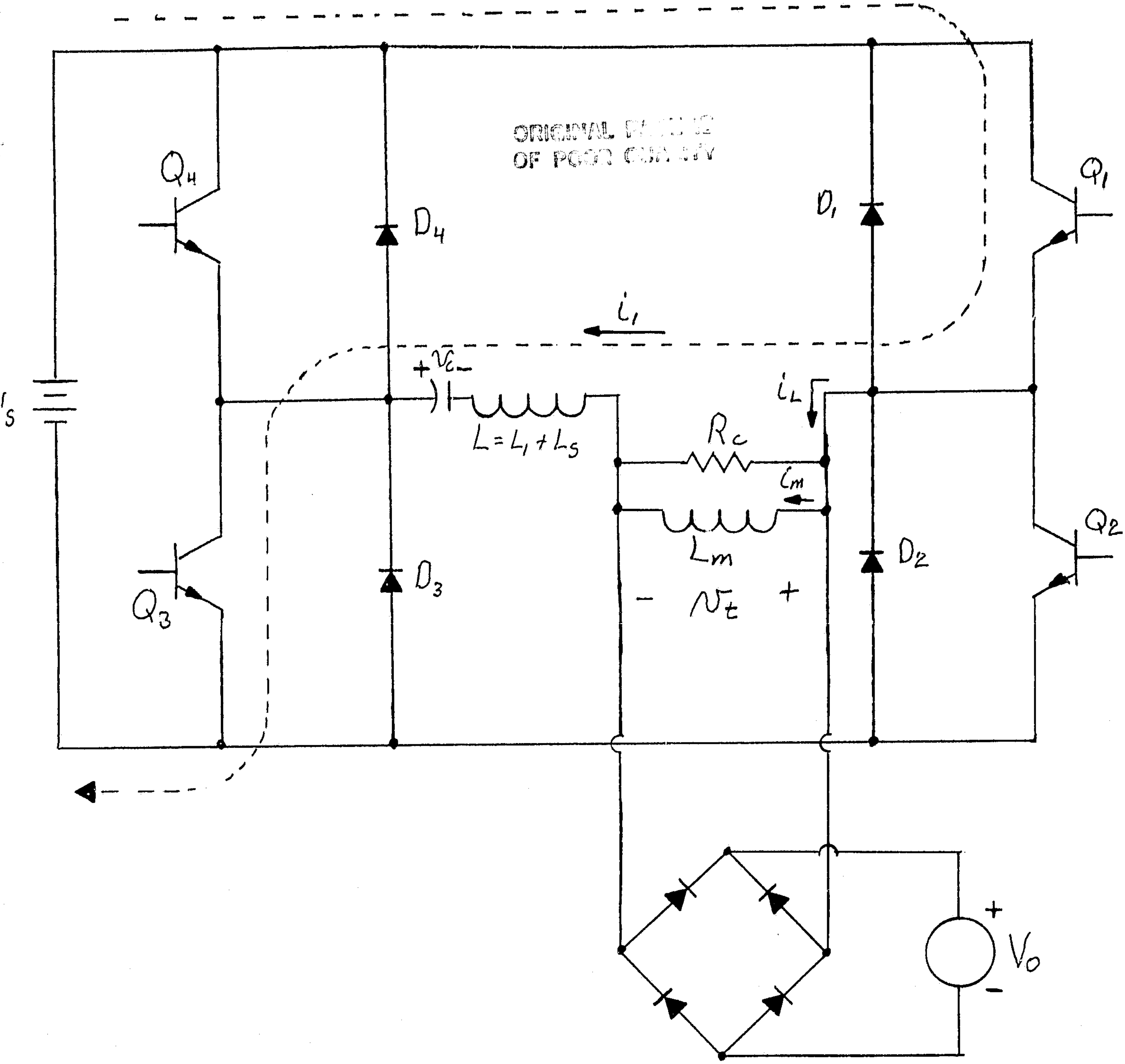


Fig. 8. Full Bridge Equivalent Circuit

And if R_c is ignored,

$$i_1(t) = \frac{V_s+V_{c2}}{Z_m} \sin \omega_m t' \quad , \quad 0 \leq t' \leq t_2'-t_2 \tag{4.}$$

where $$Z_m = \sqrt{\frac{L+L_m}{C}} \quad , \quad \omega_m = \frac{1}{\sqrt{C(L+L_m)}} \tag{5.}$$

and $$\omega_m(t_2'-t_2) = \pi \tag{6.}$$

Therefore,

$$v_c(t') = V_{c2} - \int_o^{t'} \frac{1}{C} \cdot \frac{(V_s+V_{c2})}{Z_m} \sin \omega_m t' dt' \tag{7.}$$

and $$v_c(t') = V_s(\cos\omega_m t'-1) + V_{c2}\cos \omega_m t' \quad , \quad 0 \leq t' \leq t_2'-t_2 \tag{8.}$$

Finally,

$$v_c(t_2') \equiv V_{c2}' = -2V_s-V_{c2} \tag{9.}$$

As with the half bridge circuit, we note that the effect of R_c will be to decrease $|V_{c2'}|$. Therefore assume,

$$V_{c2'} = -\psi(2V_s+V_{c2}) \quad , \quad 0 \leq \psi \leq 1 \tag{10.}$$

(ψ is defined to be the reduction factor, similar to the half bridge case)

For cyclic stability,

$$V_{c2'} = -V_{co} \tag{11.}$$

where $V_{co} = v_c(t_o)$

or

$$V_{co} = \psi(2V_s+V_{c2}) \tag{12.}$$

From [12.], we have,

$$V_{c2} = V_{co}-4V_o \tag{13.}$$

From (12.) and (13.),

$$V_{co} = 2V_o \; \psi \frac{\left(\frac{1}{q} -2\right)}{(1-\psi)} \tag{14.}$$

For the Q_1-Q_3 half cycle to proceed, we need $V_s + V_{co} > V_o$. Therefore,

$$\psi < \frac{1-q}{3q-1} \tag{15.}$$

A plot of the stable ψ vs. q region is shown in Fig. 9. As with the half bridge, the appropriate ψ is obtained by connecting an external resistance, R_{ext}, effectively in parallel with R_c as in Fig. 4. We now state,

<u>Rule F.2:</u> For .5 < q < 1.0, the full bridge converter will have cyclic stability in the discontinuous mode if $\psi < \frac{1-q}{3q-1}$ (however, the low frequency oscillation may still be present).

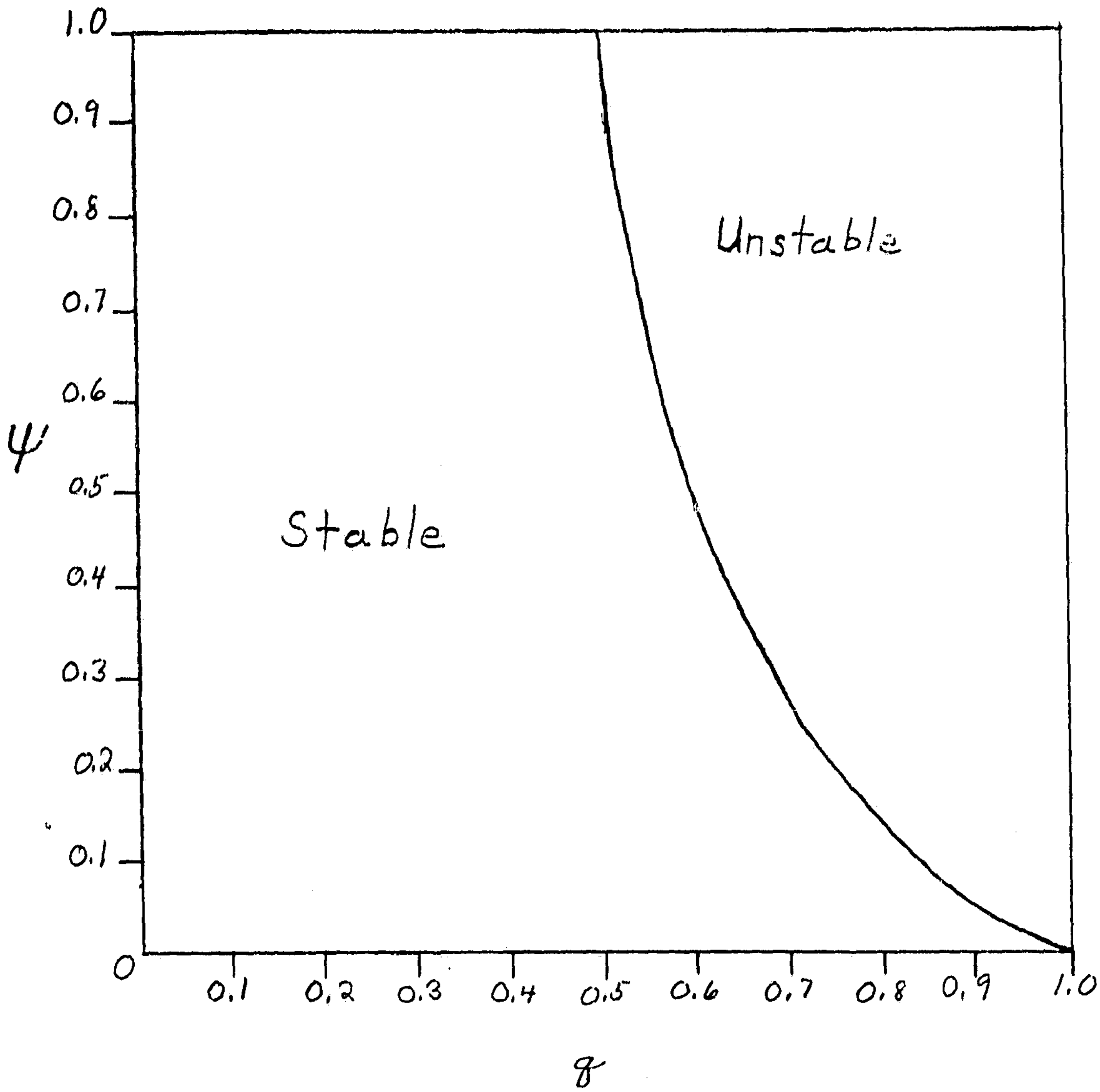


Fig. 9. Stable and Unstable ψ vs. q Regions for the Full Bridge SR Converter

Analogous to the half bridge case, this ψ factor will alter the steady state equations of [12.] for the discontinuous mode. From (14.),

$$V_{co} = 2V_s \, \psi \, \frac{(1-2q)}{(1-\psi)} \tag{16.}$$

From [12.],

$$V_{c1} = 2(V_o - V_s) - V_{co} \tag{17.}$$

where $\quad V_{c1} = v_c(t_1)$

$$\therefore V_{c1} = 2V_s \left(\frac{q-1+q\psi}{1-\psi}\right) \tag{18.}$$

Recall that for the half bridge case, a substitution of $\psi = -1$ into the V_{10} and V_{11} equations would reproduce the V_{10} and V_{11} values from [1.]. This occurs because $\psi = -1$ is equivalent to $V_{12} = V_{12'}$ for the half bridge. We see from (10.) however, that substituting $\psi = -1$ for the full bridge does not set $V_{c2'}$ equal to V_{c2}. Therefore a simple substitution of $\Psi = -1$ into (16.) and (18.) will not reproduce the original V_{co} and V_{c1} values from [12.]

From [12.], we have the following equations for $i_1(t)$ in the discontinuous mode, $\left(Z_o = \sqrt{\frac{L}{C}}\,,\ \omega_o = \frac{1}{\sqrt{LC}}\right)$,

$$i_{1(t)} = \frac{V_{co}+V_s-V_o}{Z_o}\sin(\omega_o t) \quad , \quad 0 \le t \le t_1 \tag{19.}$$

$$i_{1(t')} = \frac{V_{cl}+V_s+V_o}{Z_o}\sin(\omega_o t') \quad , \quad 0 \le t' \le t_2-t_1 \tag{20.}$$

$$\therefore I_{Q\ avg} = \frac{1}{2(\pi+\alpha)}\int_0^{\pi}\frac{V_{co}+V_s-V_o}{Z_o}\sin(\omega_o t)\,d\omega_o t = \frac{(V_{co}+V_s-V_o)}{Z_o(\pi+\alpha)} \tag{21.}$$

$$\text{and, } I_{peak} = \frac{V_{co}+V_s-V_o}{Z_o} \tag{22.}$$

If the low frequency current during $t_2 \le t \le t_2'$ is ignored,

$$I_{D\ avg} \doteq \frac{-1}{2(\pi+\alpha)}\int_0^{\pi}\frac{V_{cl}+V_s+V_o}{Z_o}\sin(\omega_o t')\,d\omega_o t' \doteq \frac{-(V_{cl}+V_s+V_o)}{Z_o(\pi+\alpha)} \tag{23.}$$

The approximate average half cycle load current on the primary is,

$$I_{avg} \doteq 2(I_{Q\ avg}+I_{D\ avg}) \doteq \frac{2(V_{co}-V_{cl}-2V_o)}{Z_o(\pi+\alpha)} \tag{24.}$$

And the approximate RMS primary load current is,

$$I_{rms} \doteq \left\{\frac{1}{\pi+\alpha}\left[\int_0^{\pi}\left(\frac{V_{co}+V_s-V_o}{Z_o}\right)^2\sin^2(\omega_o t)\,d\omega_o t\right.\right.$$

$$\left.\left.+\int_0^{\pi}\left(\frac{V_{cl}+V_s+V_o}{Z_o}\right)^2\sin^2(\omega_o t')\,d\omega_o t'\right]\right\}^{1/2}$$

$$\doteq \frac{1}{Z_o}\left\{\frac{\pi}{2(\pi+\alpha)}\left[(V_{co}+V_s-V_o)^2+(V_{cl}+V_s+V_o)^2\right]\right\}^{1/2} \tag{25.}$$

The peak capacitor voltage will occur at t_1 and t_3 where $i_1(t)$ reverses,

$$\therefore V_{c\ peak} = \pm V_{c1} \tag{26.}$$

As for the half bridge circuit, a third method for achieving cyclic stability is to lower the q value during the diode conduction intervals. As stated previously, it is preferable to implement this new q' only during the discontinuous mode, but in practice this new q' also may apply during certain continuous operating modes. Therefore the new full bridge model will assume a value of q whenever the transistors conduct and a value of q' whenever the diodes conduct. For those continuous modes where q has the same value for both transistor and diode conduction, the former model derived in [12.] still applies.

Proceeding as in [12.], the following terms are defined,

$$V_{co} \equiv v_c(0) \quad , \quad V_{c1} \equiv v_c(t_1) \quad , \quad v_{c2} \equiv v_c(t_2) \tag{27.}$$

$$\omega_o \equiv \frac{1}{\sqrt{LC}} \quad , \quad Z_o \equiv \sqrt{L/C} \quad , \quad q \equiv \frac{V_o}{V_s} \quad , \quad q' \equiv \frac{V'_o}{V_s} \tag{28.}$$

$\alpha = \omega_o(t_2 - t_1)$ where $\alpha \leq 180°$ for continuous conduction,

$$\beta \equiv \omega_o t_1, \quad t' = t_2 - t_1 \tag{29.}$$

If Q_1 and Q_3 are turned on at $t = 0$ and Q_2 and Q_4 at t_2, we have for the continuous mode,

$$i_{1(0)} \equiv I_{LO}$$

$$i_{1(t)} = I_{LO}\cos\omega_o t + \frac{V_{co}+V_s-V_o}{Z_o}\sin\omega_o t \quad , \quad 0 \le t \le t_1 \tag{30.}$$

$$i_{1(t')} = \frac{V_s+V_{c1}+V_o'}{Z_o}\sin\omega_o t' \quad , \quad 0 \le t' \le t_2-t_1 \tag{31.}$$

$$v_{c(t)} = -I_{LO}Z_o\sin\omega_o t + (V_{co}+V_s-V_o)\cos\omega_o t - V_s + V_o \quad , \quad 0 \le t \le t_1 \tag{32.}$$

$$v_{c(t')} = (V_s+V_{c1}+V_o')\cos\omega_o t' - V_s - V_o' \quad , \quad 0 \le t' \le t_2-t_1 \tag{33.}$$

Define the quantities A and B,

$$A \equiv \omega_o \int_0^{t_1} i_{1(t)}dt \quad , \quad \beta \equiv -\omega_o \int_0^{t_2-t_1} i_{1(t')}dt' \tag{34.}$$

Therefore,

$$A = I_{LO}\sin\beta + \frac{(V_{co}+V_s-V_o)}{Z_o}(1-\cos\beta) \tag{35.}$$

$$B = \frac{(V_s+V_{c1}+V_o')}{Z_o}(\cos\alpha-1) \tag{36.}$$

Now,

$$V_{c1} = v_{c(t_1)} = -I_{LO}Z_o\sin\beta + (V_{co}+V_s-V_o)\cos\beta - V_o+V_o \qquad (37.)$$

$$\therefore\ B = (1-\cos\alpha)\left(A - \frac{V_{co}+V_s+V_o'}{Z_o}\right) \qquad (38.)$$

From (35.) and (37.),

$$V_{c1} = -AZ_o + V_{co} \qquad (39.)$$

From (33.) with $\alpha = \omega_o(t_2-t_1)$,

$$V_{c2} = (V_s+V_{c1}+V_o')\cos\alpha - V_s-V_o' \qquad (40.)$$

And from (38.), (39.) and (40.),

$$V_{c2} = B\ Z_o - A\ Z_o + V_{co} \qquad (41.)$$

For cyclic stability,

$$-V_{co} = V_{12} = B\ Z_o - A\ Z_o + V_{co} \qquad (42.)$$

$$\therefore\ V_{co} = 1/2\ (A-B)\ Z_o \qquad (43.)$$

From (39.),

$$V_{c1} = -1/2\ (A+B)\ Z_o \tag{44.}$$

and from (41.),

$$V_{c2} = -1/2\ (A-B)\ Z_o \tag{45.}$$

The energy into the load during $0 \leq t \leq t_2$ is,

$$\begin{aligned} E_L &= |V_o| \int_0^{t_1} i_{1(t)}dt - |V'_o| \int_0^{t_2-t_1} i_{1(t')}dt' \\ &= \frac{|V_o|}{\omega_o} A + \frac{|V'_o|}{\omega_o} B \end{aligned} \tag{46.}$$

The energy from V_s during this period is,

$$\begin{aligned} E_s &= V_s \int_0^{t_1} i_{1(t)}dt + V_s \int_0^{t_2-t_1} i_{1(t')}dt' \\ &= \frac{V_s A}{\omega_o} - \frac{V_s B}{\omega_o} \end{aligned} \tag{47.}$$

It can be seen that the stored energy at t_2 is the same as at t_o, therefore,

$$E_s = E_L \tag{48.}$$

or from (46.) and (47.),

$$B = A\ \frac{1-q}{1+q'} \tag{49.}$$

From (38.) and (49.),

$$A\,\frac{1-q}{1+q'} = (1-\cos\alpha)\left(A - \frac{V_{co}+V_s+V'_o}{Z_o}\right) \tag{50.}$$

and from (43.),

$$A\left[\frac{1-q}{1+q'} - \frac{(1+q')(1-\cos\alpha)}{1+q'} + \frac{(q+q')(1-\cos\alpha)}{2(1+q')}\right] = -(1-\cos\alpha)\left(\frac{V_s+V'_o}{Z_o}\right) \tag{51.}$$

$$\therefore\; A = \frac{V_s}{Z_o}\left[\frac{2(1+q')^2(1-\cos\alpha)}{(q+q')-(2+q'-q)\cos\alpha}\right] \tag{52.}$$

and from (49.),

$$B = \frac{V_s}{Z_o}\left[\frac{2(1-q)(1+q')(1-\cos\alpha)}{(q+q')-(2+q'-q)\cos\alpha}\right] \tag{53.}$$

Now,

$$A-B = A\left(\frac{q+q'}{1+q'}\right) \quad , \quad A+B = A\left(\frac{2+q'-q}{1+q'}\right) \tag{54.}$$

Therefore from (43.) and (44.),

$$V_{co} = V_s\left[\frac{(q+q')(1+q')(1-\cos\alpha)}{(q+q')-(2+q'-q)\cos\alpha}\right] \tag{55.}$$

$$V_{cl} = -V_s\left[\frac{(2+q'-q)(1+q')(1-\cos\alpha)}{(q+q')-(2+q'-q)\cos\alpha}\right] \tag{56.}$$

and since the peak voltag magnitude corresponds to V_{cl},

$$V_{peak} = \pm |V_{cl}| \tag{57.}$$

For cyclic stability, note from (31.) that,

$$- I_{LO} = \frac{V_s+V_{11}+V'_o}{Z_o} \sin\alpha \tag{58.}$$

Therefore from (52.), (54.) and (56.),

$$I_{LO} = \frac{V_s}{Z_o}\left[\frac{2(1-q)(1+q')\sin\alpha}{(q+q')-(2+q'-q)\cos\alpha}\right] \tag{59.}$$

To find the angle β, note from (30.),

$$\tan\beta = \frac{-I_{LO}Z_o}{V_{co}+V_s-V_o} \tag{60.}$$

Therefore from (55.) and (59.),

$$\beta = \tan^{-1}\left\{\frac{-2(1-q)(1+q')\sin\alpha}{(q+q')(2+q'-q)-[(1+q')^2+(1-q)^2]\cos\alpha}\right\} + \pi \tag{61.}$$

The average rectified value of $i_{1(t)}$ is,

$$I_{avg} = \frac{1}{t_2}\left[\int_0^{t_1} i_{1(t)}dt - \int_0^{t_2-t_1} i_{1(t')}dt'\right] \tag{62.}$$

or from (34.),

$$I_{avg} = \frac{A+B}{\alpha+\beta} \tag{63.}$$

and from (52.) and (53.),

$$I_{avg} = \frac{V_s}{Z_o}\left\{\frac{2(1+q')(2+q'-q)(1-\cos\alpha)}{[(q+q')-(2+q'-q)\cos\alpha](\alpha+\beta)}\right\} \tag{64.}$$

The average transistor and diode currents are found in a similar manner,

$$I_{Q\ avg} = \frac{A}{2(\alpha+\beta)} = \frac{V_s}{Z_o}\left\{\frac{(1+q')^2(1-\cos\alpha)}{[(q+q')-(2+q'-q)\cos\alpha](\alpha+\beta)}\right\} \tag{65.}$$

$$I_{D\ avg} = \frac{B}{2(\alpha+\beta)} = \frac{V_s}{Z_o}\left\{\frac{(1-q)(1+q')(1-\cos\alpha)}{[(q+q')-(2+q'-q)\cos\alpha](\alpha+\beta)}\right\} \tag{66.}$$

For the RMS current we have,

$$I_{RMS} = \left\{\frac{1}{t_2}\left[\int_0^{t_1}\left(I_{LO}\cos\omega_o t + \frac{V_{co}+V_s-V_o}{Z_o}\sin\omega_o t\right)^2 dt + \int_0^{t_2-t_1}\left(\frac{V_s+V_{cl}+V'_o}{Z_o}\sin\omega_o t'\right)^2 dt'\right]\right\}^{1/2} \tag{67.}$$

$$\therefore I_{RMS} = \left\{\frac{1}{\alpha+\beta}\left[I_{LO}^2\left(\frac{\beta}{2}+\frac{\sin 2\beta}{4}\right) + \left(\frac{V_{co}+V_s-V_o}{Z_o}\right)\left(\frac{\beta}{2}-\frac{\sin 2\beta}{4}\right) + \frac{I_{LO}\left|V_{co}+V_s-V_o\right|}{Z_o}\sin^2\beta + \left(\frac{V_s+V_{cl}+V'_o}{Z_o}\right)^2\left(\frac{\alpha}{2}-\frac{\sin 2\alpha}{4}\right)\right]\right\}^{1/2} \tag{68.}$$

As in [12.], it can be shown that,

$$I_{peak} = I_{LO}\sin\beta - \frac{V_{co}+V_s-V_o}{Z_o}\cos\beta \tag{69.}$$

Comparing (35.) and (69.),

$$I_{peak} = A - \frac{V_{co}+V_s-V_o}{Z_o} \tag{70.}$$

From (52.) and (55.),

$$I_{peak} = \frac{V_s}{Z_o}\left(\frac{(1+q')^2+(1-q)^2+[(1-q)^2-(1+q')^2]\cos\alpha}{(q+q')-(2+q'-q)\cos\alpha}\right) \tag{71.}$$

When the current is discontinuous, the variables of interest can be found by substituting π for α and β in the appropriate places. Therefore from (55.) - (57.), (59.), (64.) - (66.), (68.) and (71.)

$$V_{co} = V_s(q+q') \tag{72.}$$

$$V_{c1} = V_s(-2-q'+q) \tag{73.}$$

$$V_{peak} = \pm|V_{c1}| \tag{74.}$$

$$I_{LO} = 0 \tag{75.}$$

$$I_{avg} = \frac{V_s}{Z_o}\left[\frac{2(2+q'-q)}{\pi+\alpha}\right] \tag{76.}$$

$$I_{Q\ avg} = \frac{V_s}{Z_o}\left(\frac{1+q'}{\pi+\alpha}\right) \tag{77.}$$

$$I_{D\ avg} = \frac{V_s}{Z_o}\left(\frac{1-q}{\pi+\alpha}\right) \tag{78.}$$

$$I_{RMS} = \frac{1}{Z_o}\left\{\frac{\pi}{2(\pi+\alpha)}\left[\left(V_{co}+V_s-V_o\right)^2+\left(V_{c1}+V_c+V_o'\right)^2\right]\right\}^{1/2} \tag{79.}$$

$$I_{peak} = \frac{V_s}{Z_o}(1+q') \tag{80.}$$

Consider now the restrictions on q and q' that are necessary for cyclic stability in the discontinuous mode. In order to produce the low frequency oscillation, it is necessary that,

$$V_s+V_{c2} = V_s-V_{co} = V_s\ (1-q-q') < 0 \tag{81.}$$

$$\text{or } (q+q') > 1 \tag{82.}$$

If the oscillation does occur and $R_c \approx \infty$,

$$V'_{c2} = -2V_s-V_{c2} \tag{83.}$$

Cyclic stability requires that $V'_{c2} = -V_{co}$, or,

$$V_{co} = 2V_s+V_{c2} \tag{84.}$$

From [12.], we have,

$$V_{c2} = V_{co} - 4V_o \tag{85.}$$

$$\therefore\ V_{co} = 2V_s + V_{co} - 4V_o \tag{86.}$$

which shows that the solution for V_{co} is indeterminate. This indicates that the necessary V_{co} for cyclic stability with $R_c = \infty$ cannot be found, i.e., it does not exist if $(q+q') > 1$. Therefore we must have $(q+q') < 1$, and we state,

Rule F.3: same as Rule H.3.

The same comments regarding q and q' for the half bridge also apply here, i.e., $q' = 0$ will provide stability for all $0 \leq q < 1$, but strictly speaking we only require that $0 \leq q' \leq 1-q$.

The transformer induced oscillation for the full bridge was not investigated experimentally, but it is anticipated that the results would resemble those for the half bridge due to the similarity of these two circuits.

IV. HIGHER FREQUENCY OPERATION WITH POWER MOSFETs

To establish a reference point, we will define higher frequencies to be those resonance frequencies above 100 kHz. Operating considerations can be broken down into two broad categories: 1.) circuit configuration and 2.) components. An attempt will be made to present a broad overview of design techniques and operating problems. Thus some of this information may be relatively new and some of it is already well known. The key item that permits operation in this frequency range is, of course, the power MOSFET. Efficient operation is also dependent on other techniques however, such as the use of polypropolene capacitors and magnetics using ferrite cores wound with Litz wire. Suffice it to say that many operating problems remain, and design guidelines are still lacking in certain areas. This is particularly true in the case of inductors and transformers where skin effect, proximity effects, and eddy current losses in the wire still make the design of these components an uncertain task.

The power and control circuits used in these experiments are shown in Figs. 10 and 11 respectively. The purpose of these tests was to study component stress and losses at various operating frequencies. Therefore, closed loop control was not required, and an open loop system was used to simplify the test procedure.

Power Circuit:

The power circuit in Fig. 10 is fairly straight-forward, but it is worthwhile to note a few salient features. First of all, all power MOSFETs presently available contain a parasitic anti-parallel diode that can be utilized at lower frequencies. The reverse recovery time of these diodes

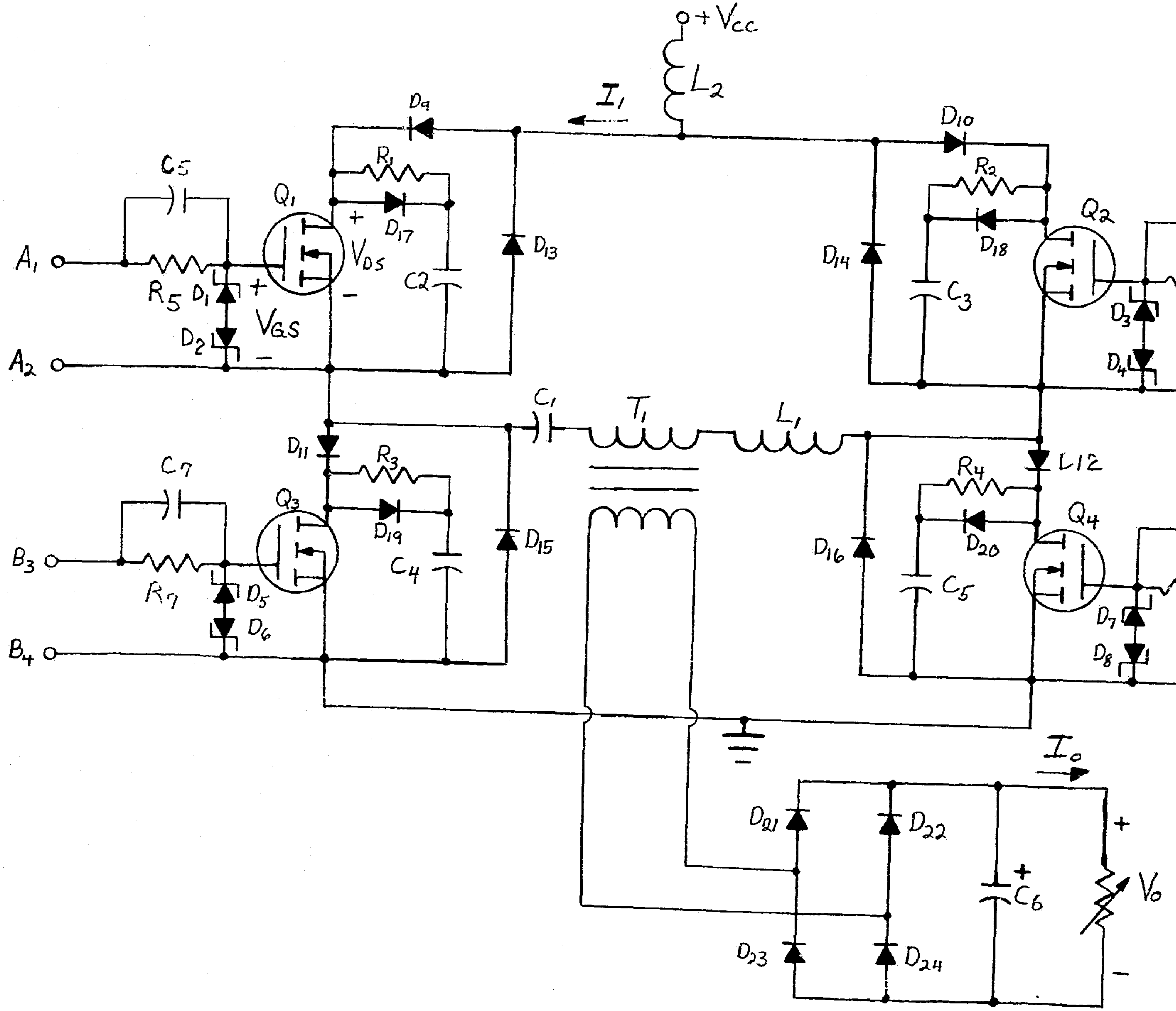


Fig. 10. Full Bridge Power Circuit

Table I: Power Circuit Parts List

$Q_1 - Q_4$:	International IRF230
$D_1 - D_8$:	1N4744
$D_9 - D_{20}$:	Motorola MR852
$D_{21} - D_{24}$:	Motorola 1N3881
C_1:	Varies with resonance frequency
$C_2 - C_4$:	Sprague 0.01μF 600V, series 715P
$C_5 - C_8$:	1500pf
C_6:	Sprague 250-200 VDC
$R_1 - R_4$:	2 Parallel 3.9k 1 watt (1.8k 2 watt)
$R_5 - R_8$:	47Ω
L_1:	Varies with resonance frequency
L_2:	14.5μH.
T_1:	Ferroxcube EC70 core; 1:1 winding ratio using 30 turns of bifilar wound 100/41 Litz wire.

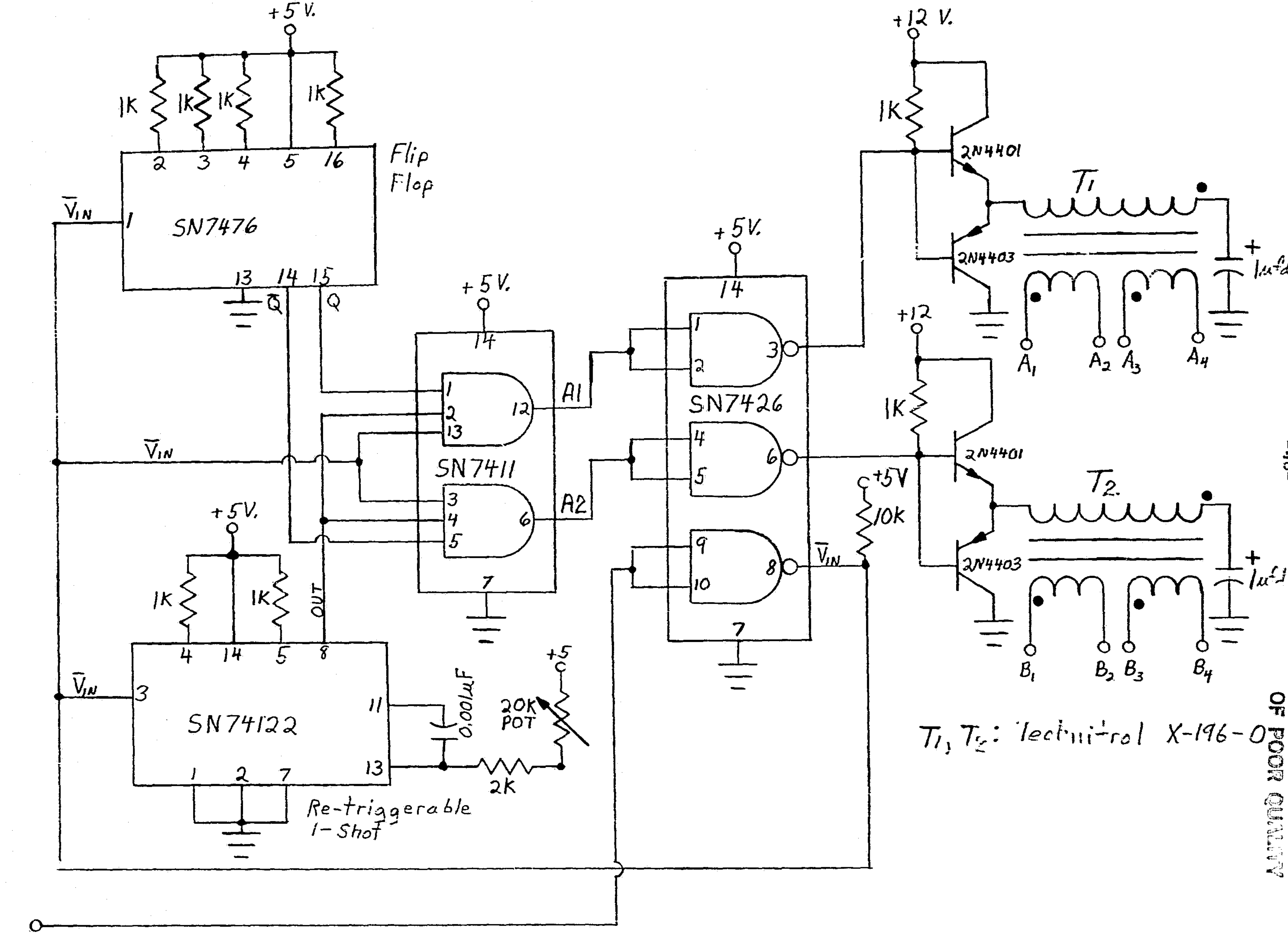
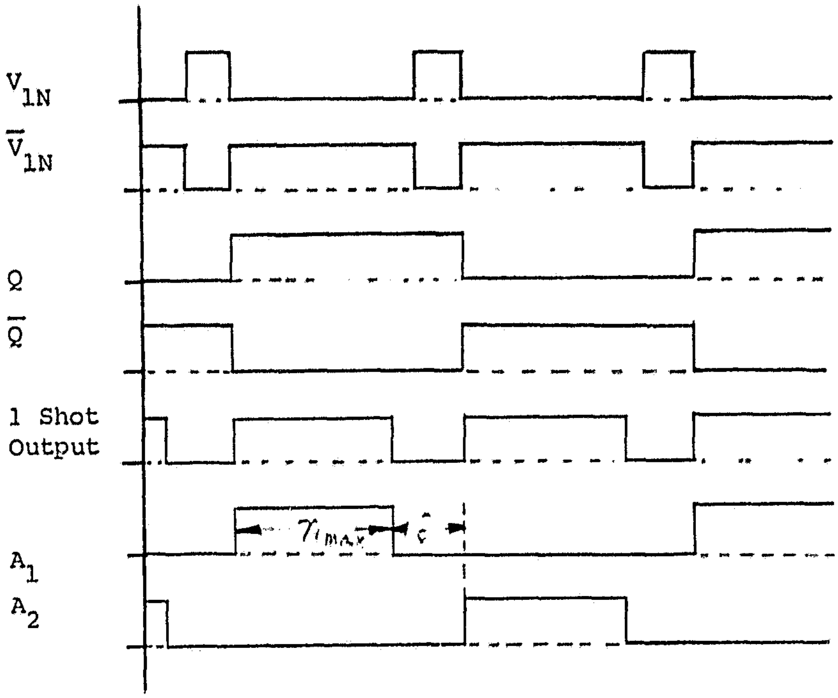
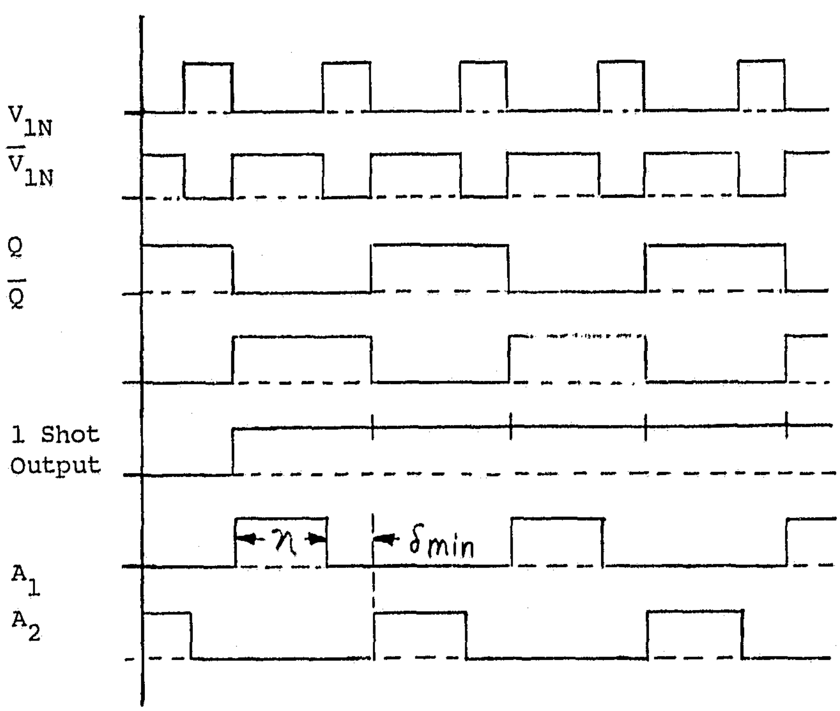


Fig. 11. Variable η and δ controller



(a.) Constant η_{max}, variable δ
(for discontinuous mode)



(b.) Variable η, constant δ_{min}
(for continuous mode)

Fig. 12. Timing Diagrams for Variable η, and δ Controller

was judged to be too slow for operation at 100 kHz. and above however, so it was necessary to bypass these parasitic diodes using D9-D16. The power MOSFETs used in these tests were the International Rectifier IRF230. The diode within this component has a specified reverse recovery time of 650 nanosec. as compared to a reverse recovery time of only 200 nanosec. for the Motorola MR852 diode. If the parasitic diode is allowed to conduct, a higher current spike will appear in the continuous mode when the diode turns off and the power MOSFET above (or below) turns on. This spike is still present even with the discrete diodes but is somewhat reduced.

Because of this current spike, it is good design practice to place a small inductor either in series with each MOSFET or in series with the source, such as L_2 in Fig. 10. In either case this inductor will see a net D.C. current (considerably higher when in series with the source) and must have an adequate air gap to prevent saturation. It should be noted that although L_2 is small in comparison to L_1, it will tend to decrease the resonance frequency. Its voltage will also add to V_{cc} over part of the cycle and may significantly increase the "off" voltage across the MOSFETs. In practice it was found necessary to adjust L_2 in concert with the MOSFET snubbers to maintain a good compromise between the current spikes and MOSFET voltages.

Another possibility for decreasing the current spike would be to slow the turn on of the on-coming MOSFET. This would allow the anti-parallel diode time to recover before the current in the MOSFET reaches a large amplitude. A potential problem with this method is that the on-coming MOSFET is being used as the current limiting device. This means that the switching interval with its high current voltage product is lengthened, and the MOSFET's

switching losses may increase (even though the current spike is decreased).

At these resonance frequencies, the leakage inductance of T_1 can be significant in comparison with L_1. Thus close coupling is required between the primary and secondary windings of T_1 to prevent the leakage inductance from exceeding the total value required at the desired resonance frequency. One attractive possibility might be to depend entirely on the leakage inductance and dispense with L_1 altogether. Such a transformer may be difficult to build however since the leakage inductance must be some specific low value. A flux shunt design requires that primary and secondary windings must be on separate legs of the core, which means that the minimum possible leakage inductance may still be too high.

Control Circuit:

As stated previously, an open loop system was used in these tests in order to simplify the control circuitry. Furthermore, it was decided to use a variable frequency drive signal that does not have to be sychronized with the zero crossings of the load current. Such a system is relatively easy to implement and can be adapted to a closed loop system by using a voltage controlled oscillator (VCO) in the feedback loop.

Since the drive signal is not synchronized to the resonance frequency it must meet some rather specific requirements. First of all for the on angle, η, we must always have,

$$\eta > \beta$$

where β = MOSFET conduction angle. Next, we must have some finite off angle, $\delta > 0°$, in between the two drive signals to prevent simultaneous turn on of

two MOSFETs in series. Fig. 13 shows the discontinuous and continuous mode control signals for two different strategies,

1. Constant η ($\eta > 180°$), variable δ.

2. Variable η and δ.

If the constant η version is used, η must be slightly greater than 180° which is the maximum MOSFET conduction angle. For example, if the MOSFET turn-on delay angle were 10 degrees and a 10 degree safety margin was desired at the end of the pulse, η = 200 degrees. Therefore over a complete conduction interval, $2\eta + 2\delta = 2\gamma$, where γ is the conduction angle for 1/2 cycle. Suppose we specify δ_{min} = 10 degrees,

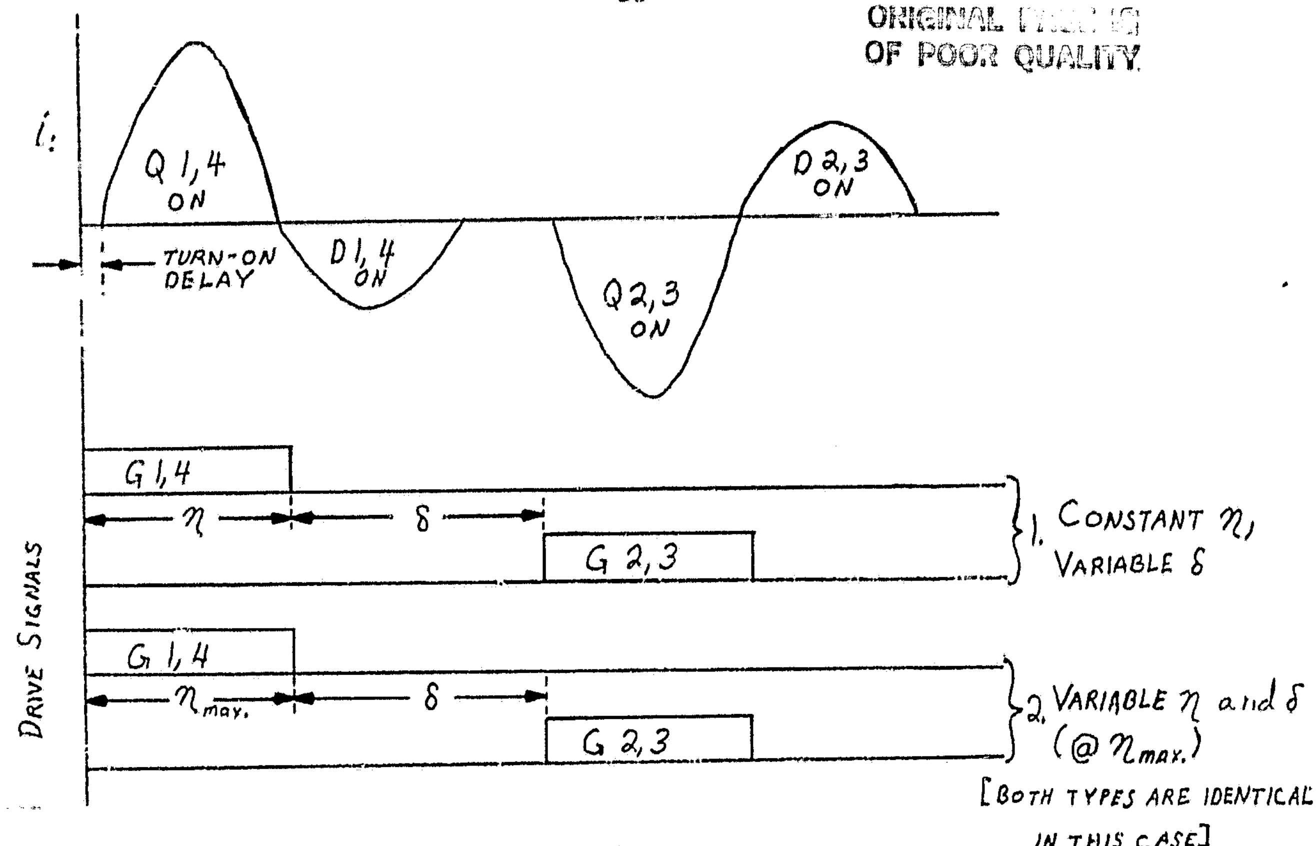
$$\therefore \quad 2(200) + 2(10) = 2\gamma$$

$$\gamma_{min} = 210°$$

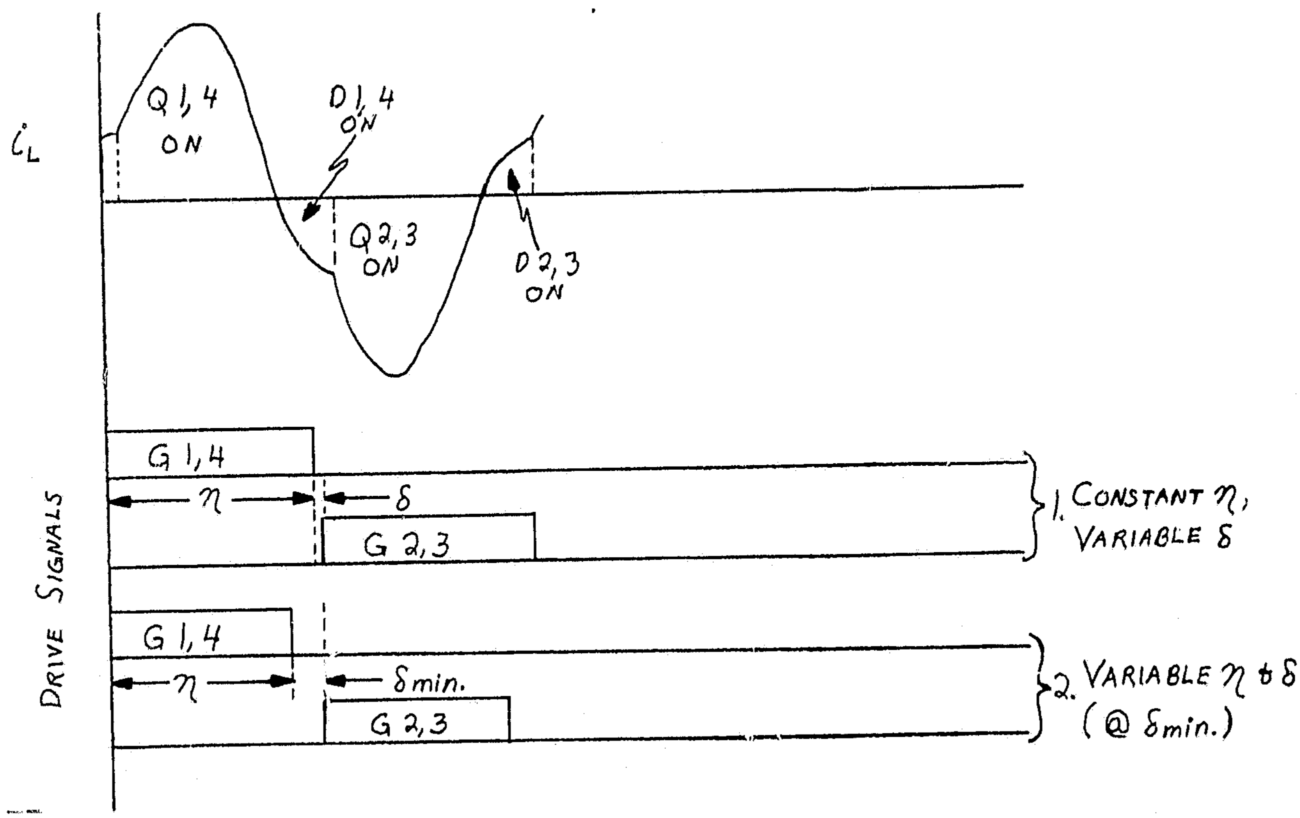
Referring to Fig. 14 (which is derived from the formula, $\gamma = \alpha + \beta$), at $q = .9$,

$$\gamma_{min} = 210° \Rightarrow \alpha_{min} = 44°$$

From Fig. 15 the normalized average load current, $I_{AN} = 1.6$ @ $\alpha_{min} = 44°$. The value of $I_{AN} = 1.6$ represents a severe limit on the maximum output current (and of course, power). For example, if α_{min} could be decreased to 35°, $I_{AN} = 2.4$ which represents a 50% power increase.

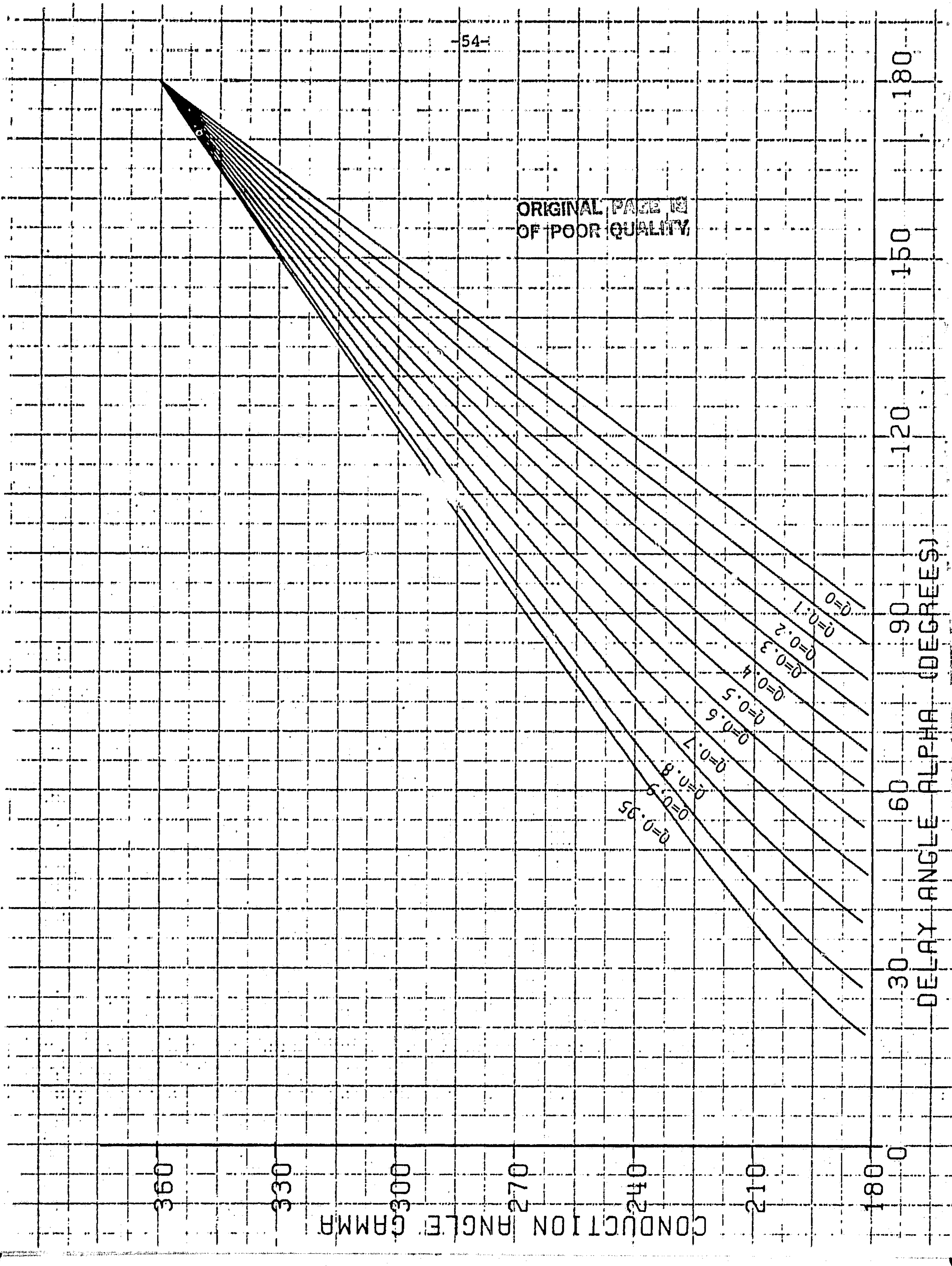


(a.) Discontinuous Mode



(b.) Continuous Mode

Fig. 13. Load Current and Control Signals using
1. Constant η, variable δ and
2. Variable η and δ


DELAY ANGLE ALPHA (DEGREES)
0
30
60
90
120
150
180
CONDUCTION ANGLE GAMMA
360
330
300
270
240
210
180
Q=0
Q=0.1
Q=0.2
Q=0.3
Q=0.4
Q=0.5
Q=0.6
Q=0.7
Q=0.8
Q=0.9
Q=0.95

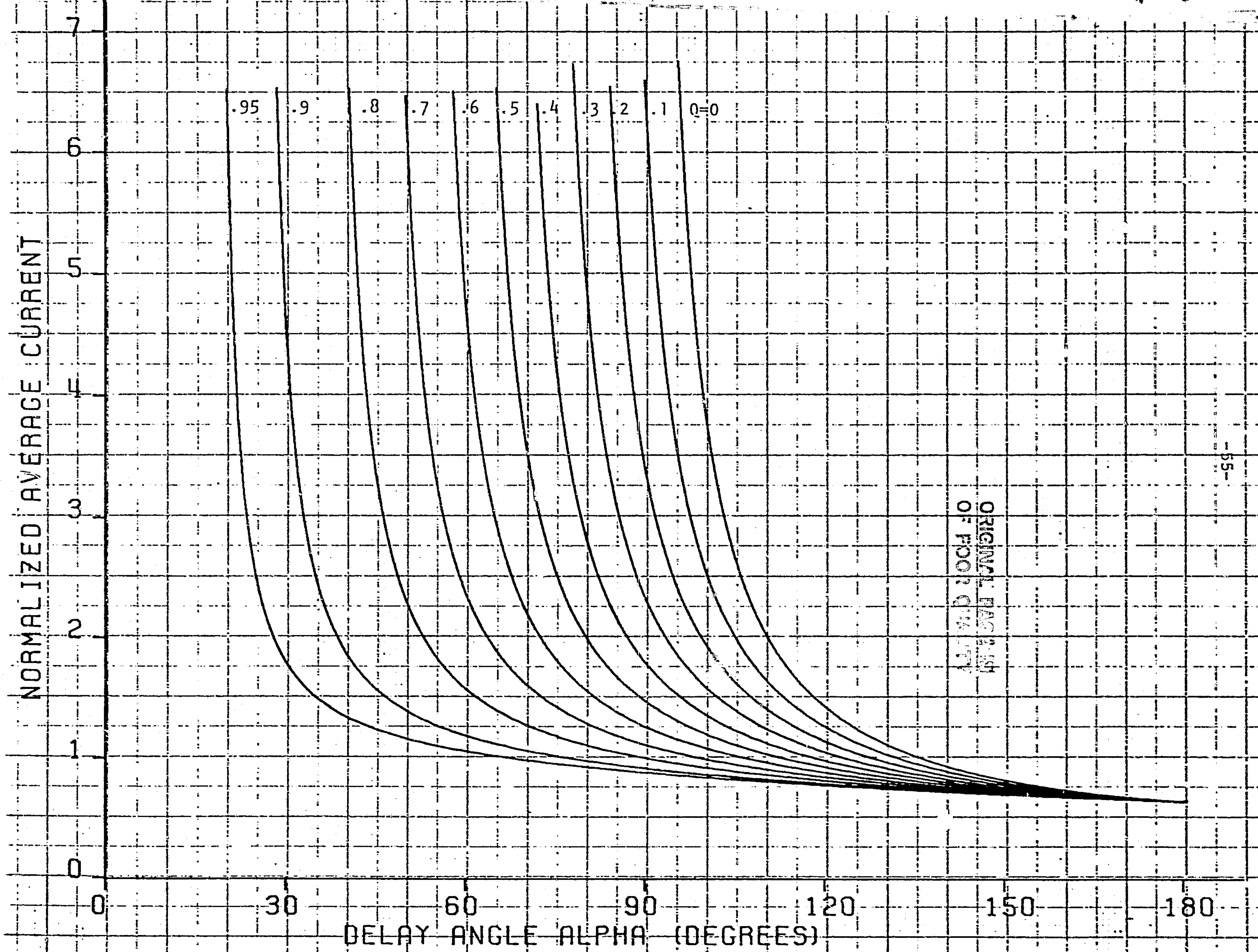


Fig. 15. Normalized Average Current, I_{AN}, vs. α

Instead, suppose we chose the variable η and δ arrangement. In this case η varies in the continuous mode, but δ is held constant at some δ_{min}. Conversely, in the discontinuous mode η is held constant at some $180° < \eta < 360°$, but δ varies.

Suppose we wish to use $\alpha_{min} = 35°$ (which was not obtainable with the constant η controller) and the same $\delta_{min} = 10°$.

From Fig. 14 at $q = 0.9$, $\gamma_{min} = 196.5°$

$$\therefore 2\eta + 2\delta = 2\gamma$$

$$2\eta + 2(10°) = 2(196.5°)$$

$$\therefore \eta = 186.5°$$

$$\beta = \gamma - \alpha = 196.5° - 35° = 161.5°$$

$\therefore$ turn on delay + safety margin $= \eta - \beta = 186.5° - 161.5° = 25°$, which is above the minimum allowable value of 20°.

The schematic for the variable η and δ controller used in these tests is shown in Fig. 11. Fig. 12 shows two typical timing diagrams for this circuit. The circuit can be operated open loop by connecting V_{1N} to variable frequency pulse generator with a fixed on time, or it can be operated closed loop by connecting V_{1N} to a voltage controlled oscillator (VCO).

Power MOSFET's:

Obviously, the key component that permits operation at frequencies above 100 kHz is the power MOSFET. The advantages of this device, such as low drive current requirements, ease of paralleling, and high switching speeds are well known and will not be elaborated here. As mentioned previously,

the parasitic anti-parallel diode of the power MOSFET is too slow for this application and must be isolated by D9-D16 in Fig. 10. In regard to switching speed, the power MOSFET should have a turn-off delay time ($t_{d(off)}$ that is less than the minimum conduction time of the anti-parallel diode. The International Rectifier IRF230 MOSFET's used in these tests had a maximum $t_{d(off)}$ = 100 ns. Fall time, t_f, is not as critical in this application since the MOSFET initiates the turn-off process when the drain-source current is already zero.

In this type of series resonant circuit the turn-on switching losses of the MOSFET (or any type of switch) are much more critical than the turn-off switching losses. This is because in the continuous mode the MOSFET must rapidly pick-up the previously conducting diode current, whereas at turn-off the MOSFET current is zero. Thus fast turn-on time becomes quite important to reduce switching losses, as was explained in the section describing the power circuit. The IRF230's used in these tests have a maximum turn-on delay time $t_{d(on)}$ = 50 ns and a maximum rise time t_r = 140 ns (which is the more important of the two since it is during this time that high voltage x current products will occur).

Diodes and Rectifiers:

As mentioned previously, the parasitic diode within the MOSFET is too slow for this application and must be isolated, e.g., using D9 and D13 for Q_1 in Fig. 10. Naturally, D13 should be as fast as possible. These tests used Motorola MR852's having a t_{rr} = 200 ns. The speed of the blocking diodes, D9 - D11, is not as critical, but MR852's were used here also. It may be possible to use slower diodes for D9 - D11, but this was not evaluated experimentally. The snubber diodes D17 - D20 should be fast to minimize the

snubber capacitor discharge spike, so MR852's were also used here. Likewise high speed diodes should be used for the rectifier bridge D21-D24, so Motorola 1N3881's with t_{rr} = 200 ns were selected.

Power Circuit Capacitors:

The combination of high frequency and current requires capacitors with a very low dissipation factor for both the resonant capacitor, C1, and the snubber capacitors C2 - C5. These tests use the Sprague Type 715P series which has a polypropylene plastic-film dielectric. These units appeared to be satisfactory and did not exhibit any noticeable heating. Sprague only provides voltage ratings up to 20 kHz. for these units (490 V. A.C. RMS @ 20 kHz. for a 1600 V.D.C. unit of .0018 to .10 ufd.), but no failures were experienced.

Power Circuit Inductors and Transformers:

Initially an attempt was made to construct these components using ferrite pot cores and standard magnet wire. This proved to be totally unsatisfactory, even at 100 kHz., the lowest frequency tested. Losses were not measured, but they were so excessive that virtually no output power was obtained, and the windings and bobbins were damaged by heating.

To allow more cooling and to minimize core loss, Ferroxcube ED70-3C8 ferrite cores were used for both the resonant inductor and the output transformer. This is an "E" type core with a rounded center leg. It allows better cooling than the pot core and uses a round bobbin for easier winding and lower leakage inductance. The 3C8 core material also appears to have about the

lowest losses that are commercially available at frequencies and flux densities used in this application.

It was also necessary to use Litz wire in all of these magnetic components to counteract the rather high losses in the wire due to skin effect, eddy currents, and proximity effect. Litz wire is available in a very wide variety of wire sizes and number of strands, but very little technical literature is available as to which combination should be selected for a given frequency and/or flux density. Because of this lack of information, it was necessary to resort to some experimental tests, and these yielded some rather interesting results.

The test circuit is shown in Fig. 16. Power losses were measured with a Clark-Hess Model 255 wattmeter, which is very inaccurate at low power factors. Therefore it was necessary to measure the losses using an LC resonance circuit to achieve a high power factor. Thus the loss measurements also include those of the capacitor. However, even if capacitor losses are significant they should be the same for each inductor tested since the inductance values were all equal. All measurements are made in the following manner. With a given number of turns on the inductor, the air gap is adjusted until the tank circuit resonates at the test frequency. This is evidenced by obtaining the minimum resonance current. The voltage amplitude from the amplifier is then adjusted to provide an inductor current of 8 amps peak. A series resonance circuit would be a better simulation of the converter, but the amplifier could not supply the required 8 amps peak. Because of the high voltage across the resonance circuit it was necessary to use the 1000 volt

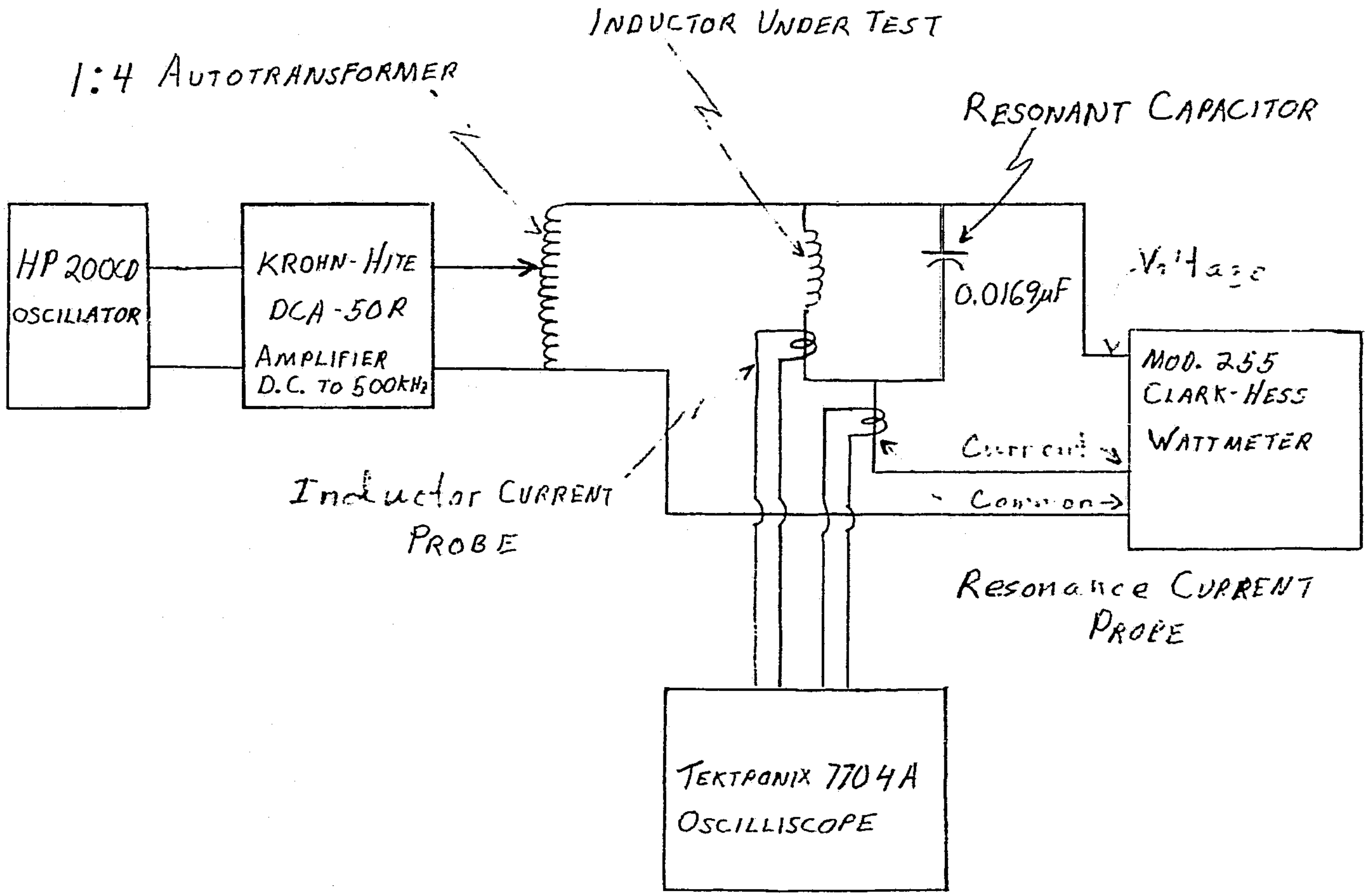


Fig. 16. Resonant Inductor Test Circuit

scale of the wattmeter. The accuracy of this scale is only specified fo frequencies less than 200 kHz. however, so some error is introduced at higher frequencies.

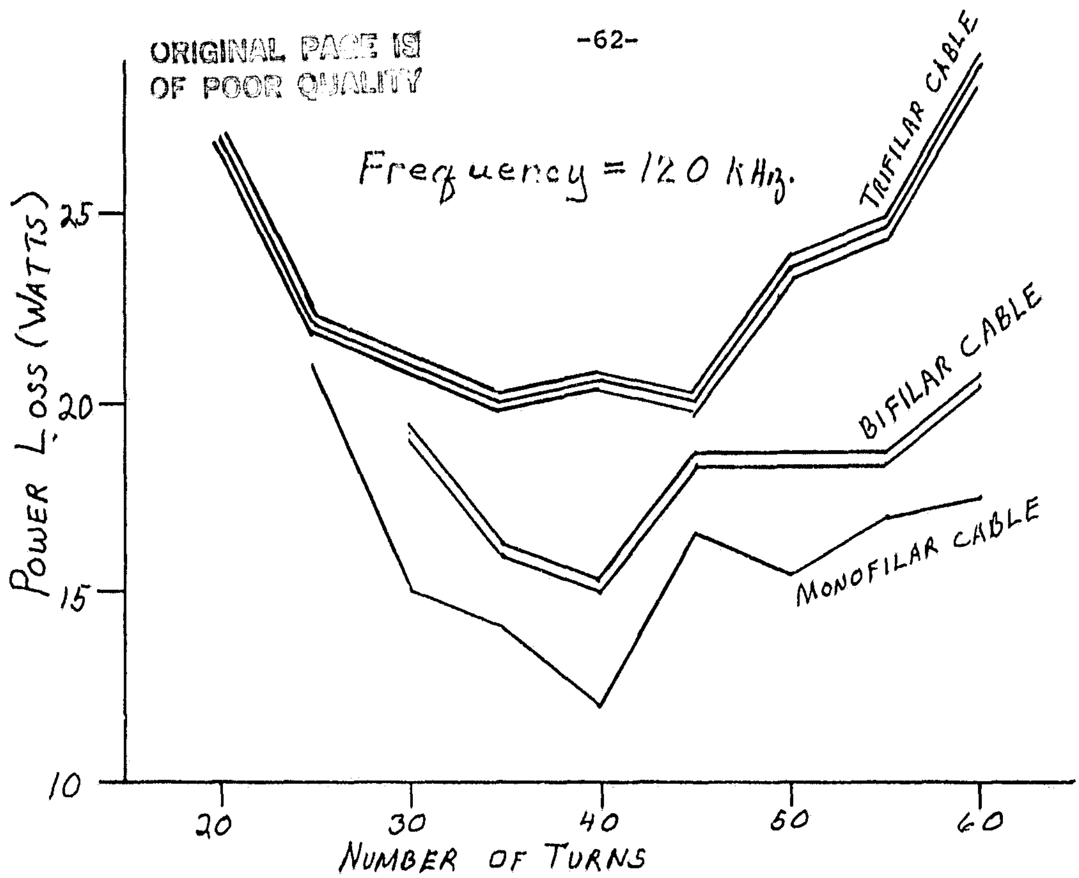
Fig. 17 shows the results using Litz wire consisting of 50 strands of no. 36 wire (50/36). Two interesting results should be noted:

1. Losses increased as the number of wires increased.

2. There appears to be an optimum number of turns (different combinations of turns and air gaps were used to achieve the same inductance).

The fact that the losses increase with the amount of copper seems to indicate that losses in the wire due to eddy currents and proximity effect are more significant than conventional resistive losses. Fig. 18 shows some data using fewer strands of larger gauge wire. The trend in Fig. 18 is generally consistent with that of Fig. 17, although the results for 5/21/33 (5 twisted cables each with 21 strands of no. 33) were about the same as those for 15/30 below 45 turns. Obviously, the losses will eventually reach a minimum and then start to increase with further decreases in wire area. This point was not determined in these tests however due to time and budget constraints (Litz wire tends to be quite expensive and off-the-shelf values are limited).

Fig. 19 shows a side view of the typical construction for one of these resonant inductors. Since it was necessary to vary the air gap for different tests, the same gap is present in all three legs and is maintained by spacers in the two outer legs. This is in contrast to the usual practice of gapping only the center leg. This particular construction may produce additional



a.) Losses vs. number of turns on inductor

No. Turns	Power Loss			Air Gap (mm)		
	No. Cables			No. Cables		
	1	2	3	1	2	3
60	17.5	20.5	29.0	14.0	15.5	15.5
55	17.0	18.5	24.5	10.5	12.0	12.0
50	15.5	18.5	23.5	8.5	10.0	10.0
45	16.5	18.5	20.0	7.0	7.5	8.0
40	11.5	15.0	20.5	6.0	5.0	6.5
35	14.0	16.0	20.0	6.0	3.8	4.0
30	15.0	19.0	19.5	4.0	2.0	2.5
25	21.0		22.0	2.5		1.5

b.) Losses and air gap vs. number of turns

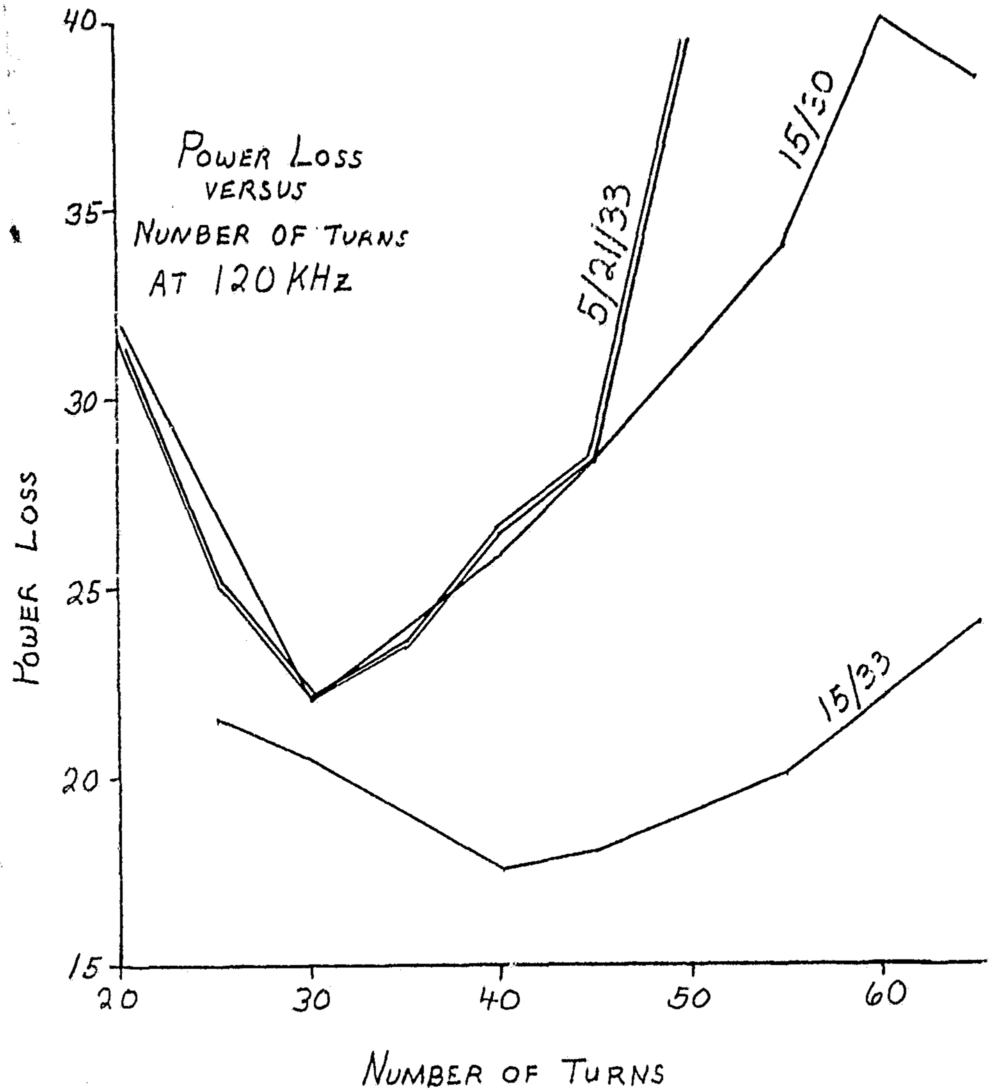
Notes: 1. Core - Ferroxcube EC703C8 ferrite, Cable - 50/36 SPSN Litz wire

2. L is tuned to resonate with C = .0169μfd. @ 120 kHz.

3. Inductor current - 8 amps peak.

Fig. 17. LC Resonance Circuit Loss Data with Parallel Cables.

Test Circuit is shown in Fig. 16.



No. Turns	Wire Types 15/30	15/33	5/21/33
65	38.5	24.0	
60	40.0	22.0	
55	34.0	20.0	
50	31.5	19.0	39.5
45	28.5	18.0	28.5
40	26.0	17.5	26.5
35	24.0	19.0	23.5
30	22.0	20.5	22.0
25	26.5	21.5	25.0
20	32.0		31.5

Losses in watts

Fig. 18. LC Resonance Circuit Loss Data for Different Types of Litz Wire. Test Circuit is shown in Fig. 16.

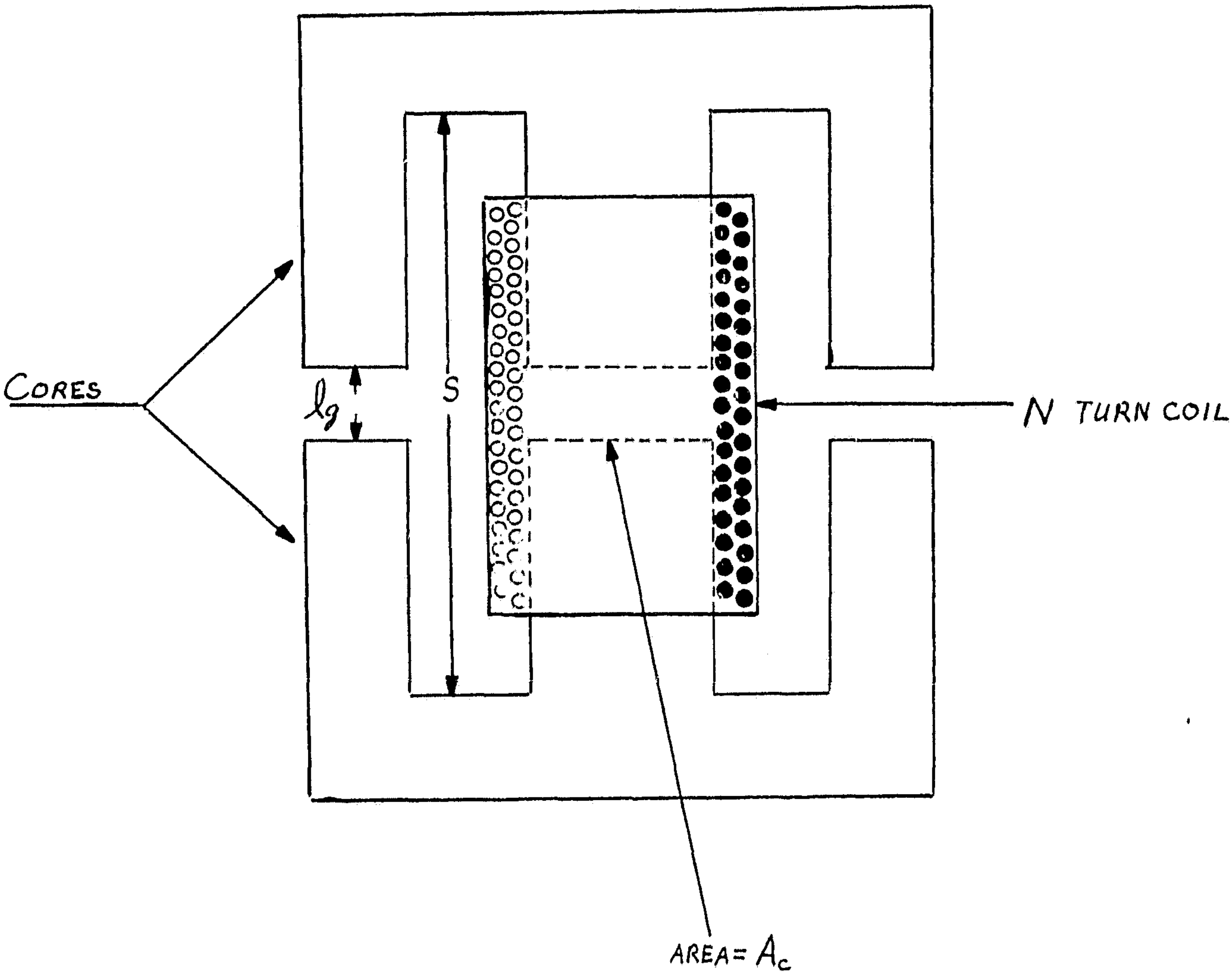


Fig. 19. Resonance Inductor Construction using EC Type Ferrite Cores

fringing effects since the gaps are fairly long and the two outer gaps are not within the coil, but there appeared to be no practical way to avoid this. In standard ferrite E cores, the cross sectional area of each outer leg is usually 50% of that of the inner leg. This does not appear to be exactly the case for the EC core, since the outer area is somewhat greater than 50% of the inner one. However, for the sake of convenience, a 50% relationship will be assumed.

If fringing flux is taken into account [21, 22],

$$B_{max} = \frac{0.5\ N\ I_{max}}{l_g} \cdot \left(\frac{L'}{L}\right) \quad \text{Gauss}$$

where $$\frac{L'}{L} = \left(1 + \frac{2\ l_g}{\sqrt{A_c}}\ \ln \frac{25}{l_g}\right)$$

N = number of turns

$\frac{l_g}{2}$ = length of each gap (in.)

A_c = cross sectional area (in.^{2})

S = (see Fig. 19). (in.)

If the above equations are applied to the 40 turn, single cable inductor in Fig. 17 we have,

$$\frac{L'}{L} = \left(1 + \frac{2(0.47)}{\sqrt{.43}}\ \ln \frac{2(2.03)}{0.47}\right) = 4.09$$

$$B_{max} = \frac{0.5x40x8x4.09}{0.47} = 1393 \text{ gauss}$$

@ 120 kHz., core losses for Ferroxcube 3C8 ferrite ≈ 110 mw./cm.^{3},

volume for EC70 core = 40.1 cm.^{3}

∴ core loss ≈ 4.4 watts.

The total loss at this point is 11.5 watts (which also includes capacitor losses). Therefore we have, wire + capacitor loss = 11.5 - 4.4 = 7.1 watts.

Repeating the above procedure for 25 and 60 turns, we have

Turns	B_{max} (gauss)	Core loss (watts)	Capacitor + wire loss (watts)
25	1687*	4.8	16.2
40	1393	4.4	7.1
60	1279	4	13.5

*for small gaps, [21] suggests using $B_{max} = \frac{0.6\ NI_{max}}{l_g} \left(\frac{L'}{L}\right)$

Although the exact reasons for this behavior have not been verified, it appears that the wire losses are directly related to both B_{max} and the copper mass. Since these two quantities vary in opposite ways with respect to the number of turns, it is then possible to find a minimum loss point, e.g., 40 turns in this case.

Whatever the reasons for this behavior, there appears to be no known way of predicting the optimum number of turns or the losses in advance. This

means that optimum inductor design becomes an experimental procedure at these frequencies. Although such a procedure is feasible, it would certainly be preferable to have a more accurate model that would provide an analytical design.

Circuit Performance:

In order to investigate the converter's characteristics at higher frequencies, circuits were built and tested at resonance frequencies of 120, 200 and 300 kHz. The purpose of these tests was only to investigate the feasibility of higher frequency operation and to identify potential operating problems. Thus, the cirucits were operated open loop for simiplicity, and problems such as packaging and cooling were not considered. As expected, the maximum output power and efficiency tended to decrease with increasing frequency. Fig. 20 gives an indication of this for the three resonance frequencies tested. The efficiency values in Fig. 20 do not include losses in the control circuit and thus are somewhat higher than those for the complete circuit. The reason for taking this approach was that all efforts to improve efficiency were concentrated on the power circuit, where most of the losses will occur. Even on this basis, the efficiencies tended to be low in comparison to previous results at lower resonance frequencies. Table 2-IV of [23.] for example, reports a thyristor 20 kHz half bridge circuit with a power stage efficiency of 88% and a transistor 50 kHz full bridge circuit with a power stage efficiency of 87.2%. It is felt that additional design experience could decrease the power circuit losses somewhat, but it may be difficult to match the efficiencies obtained at lower resonance frequencies. As mentioned earlier, the design of the output transformer and resonance inductor is one

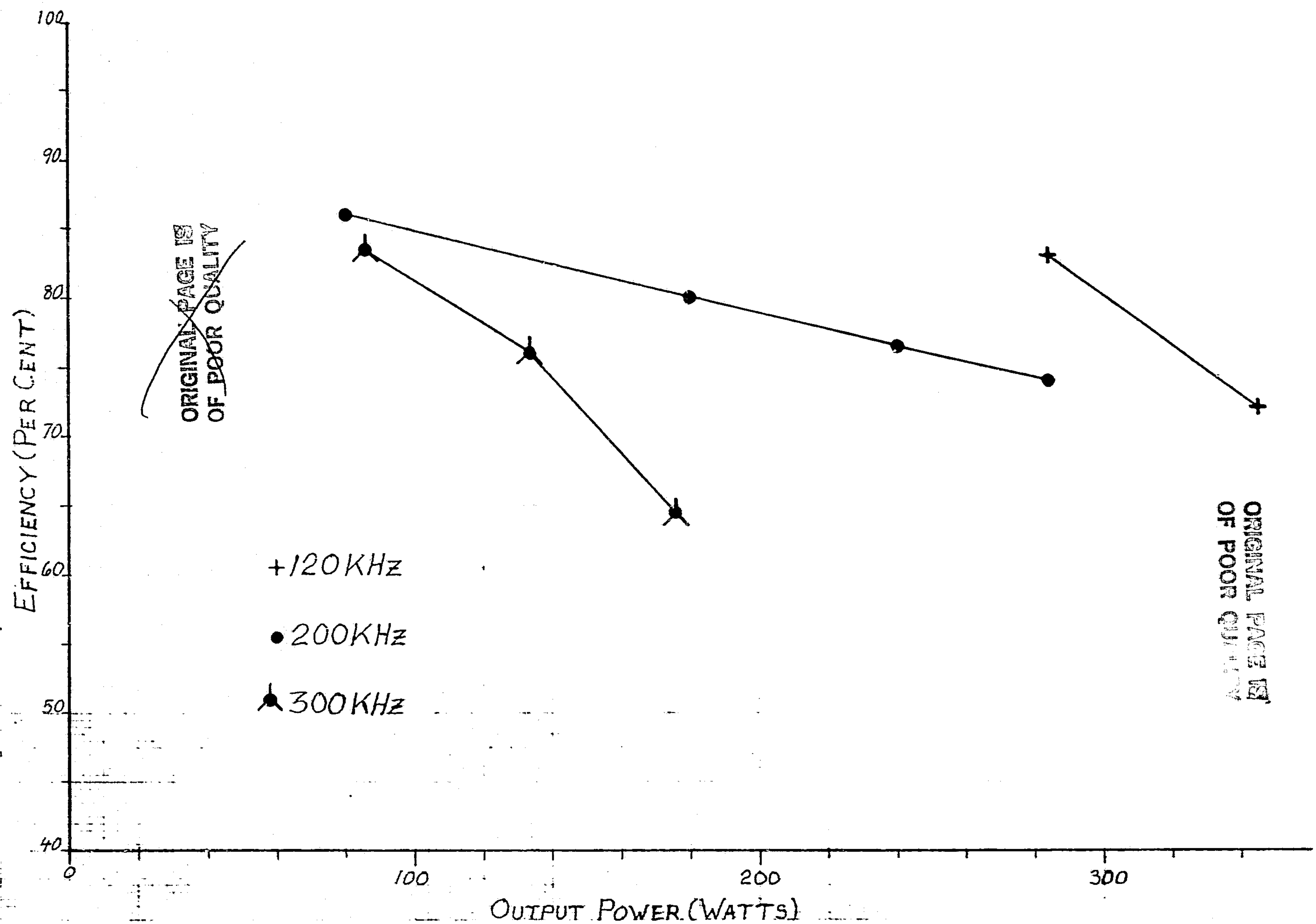


Fig. 20. Power Circuit Efficiency vs. Output Power for Resonance Frequencies of 120, 200 and 300 kHz

particular area where it may be possible to further decrease circuit losses.

Fig. 21 shows the V_{DS} and I_1 (Fig. 10) waveforms for the 120 kHz resonance circuit in the continuous current mode. The relatively long rise and fall times of I_1 are largely due to the commutating choke, L_2, in Fig. 10. This choke is intended primarily to limit the recovery current spike that occurs after the diode conduction interval.

Figs. 22-24 show the I_1 and V_{DS} waveforms for continuous current under various operating conditions. Fig. 22 is an example of the higher efficiencies that are possible at lower loads and higher q values. Figs. 23 and 24 illustrate the effect of the commutating choke, L_2. As seen from the I_1 waveforms, the recovery current spike is considerably higher without L_2.

Figs. 25 and 26 show various waveforms for the continuous current mode at a resonance frequency of 300 kHz. This was the highest frequency used in these tests due to the decreasing efficiencies at higher frequencies. It is also interesting to note the severe distortion in I_1 at $P_o \approx 170$ watts in Fig. 26.

These tests indicate that it is at least feasible to operate these circuits up to 300 kHz., but the efficiencies in this frequency range are presently too low for most applications. Operation at some frequency above 100 kHz. may be practical however, and it would be worthwhile to study this possibility further. To be truly definitive, studies of this type should consider the entire circuit package, including cooling requirements. It may well be that the maximum power/weight ratio for MOSFET converters occurs at some frequency well beyond that for thyristor or bipolar transistor versions.

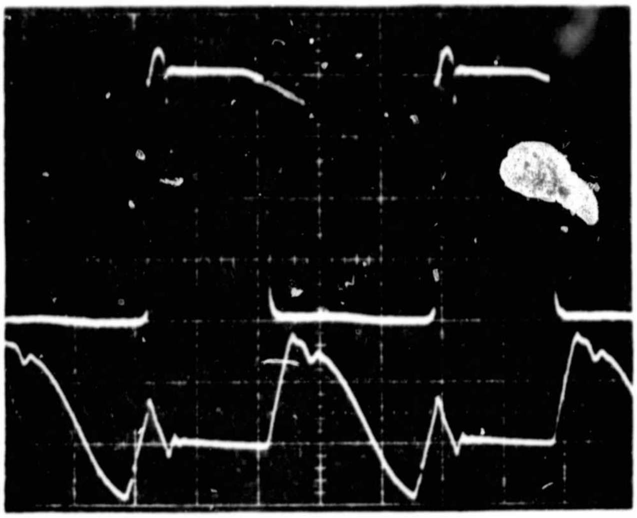


Fig. 21. V_{DS} and I_1 for the circuit in Fig. 10.
f_o = 120 kHz., time scale = 2μs./cm.
Top: V_{DS}, 50V./cm., Bottom: I_1, 4A./cm.
V_o = 75V., I_o = 4.6A., P_o = 345ω., q = 0.56,
efficiency = 73%.

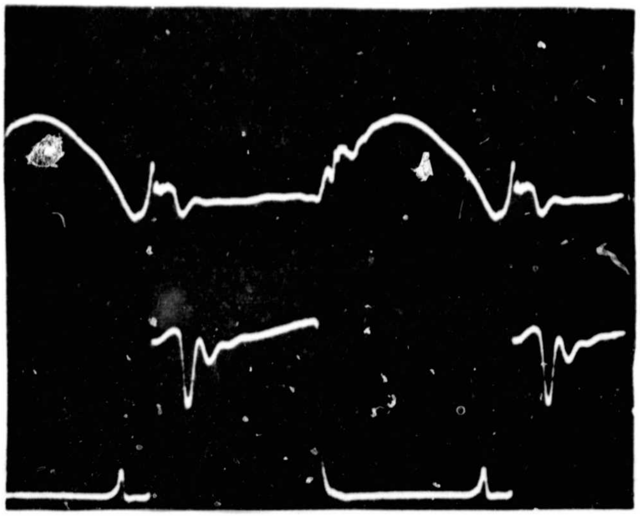


Fig. 22. V_{DS} and I_1 for the circuit in Fig. 10.
f_o = 200 kHz., time scale = 1μs./cm.
Top: I_1, 2A./cm., Bottom: V_{DS}, 50V./cm.
V_o = 95V., I_o = 1.9A., P_o = 180ω., q = 0.78,
efficiency = 80%

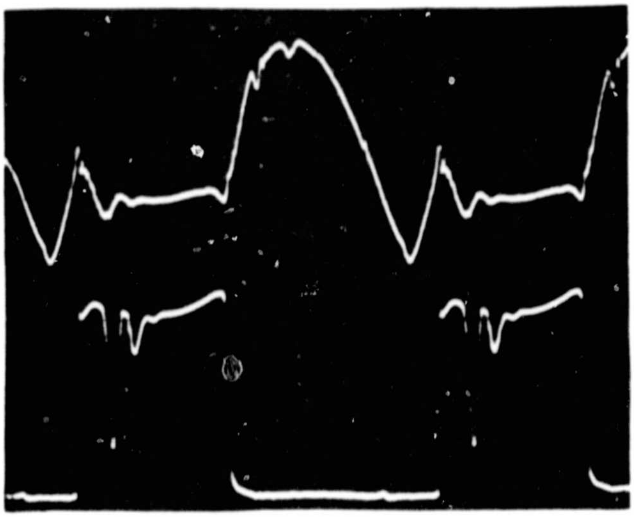


Fig. 23. V_{DS} and I_1 for the circuit in Fig. 10.
f_o = 200 kHz., time scale = 1μs./cm.
Top: I_1, 2A./cm., Bottom: V_{DS}, 50V./cm.
V_o = 80V., I_o = 3.55A., P_o = 284ω., q = 0.66,
efficiency = 74%

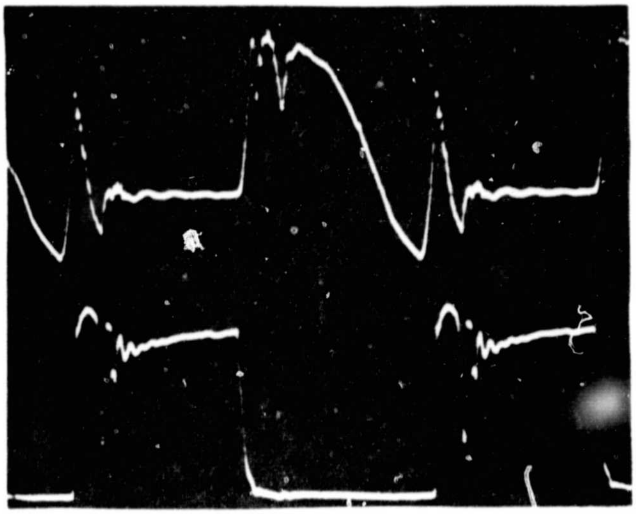


Fig. 24. V_{DS} and I_1 for the circuit in Fig. 10 without L_2.
f_o = 200 kHz., time scale = 1μs./cm.
Top: I_1, 2A./cm., Bottom: V_{DS}, 50V./cm.
V_o = 74V., I_o = 3.25A., P_o = 240ω., q - 0.61,
efficiencv = 72%

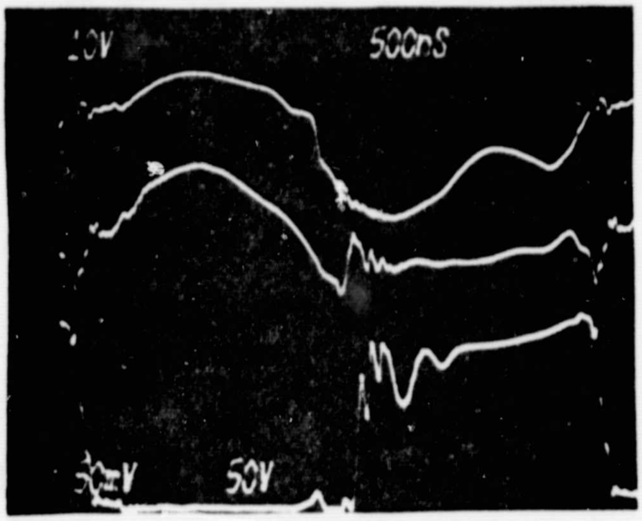


Fig. 25. V_{GS}, I_1 and V_{DS} for the circuit in Fig. 10.
f_o = 300 kHz., time scale - 500 ns./cm.
Top: V_{GS}, 10V./cm., Center: I_1, 1A./cm.
Bottom: V_{DS}, 50V./cm.
V_o = 90V., I_o = 1.2A., P_o = 135ω., q - .77,
efficiency = 77%

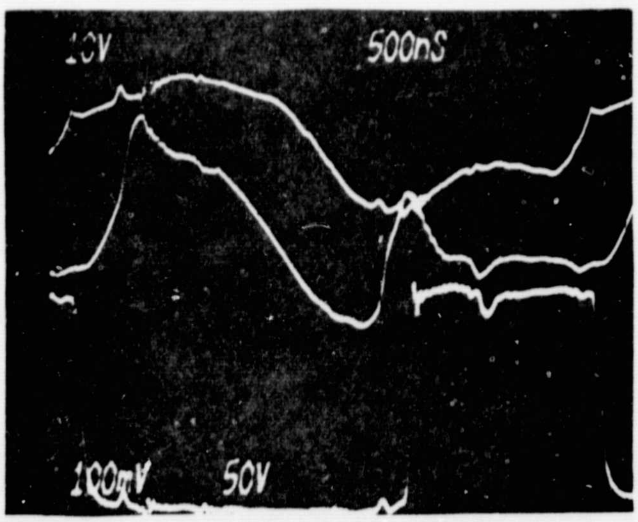


Fig. 26. V_{GS}, I_1 and V_{DS} for the circuit in Fig. 1C.
f_o = 300 kHz., time scale - 500 ns./cm.
Top: V_{GS}, 10 V./cm., Center: I_1, 2A./cm.,
Bottom: V_{DS}, 50V./cm.
V_o = 65V., I_o = 2.7A., P_o = 175ω., q = 0.53,
efficiency = 65%

V. SUMMARY AND FUTURE WORK

The main goals of this research were to investigate 1.) a low frequency oscillation induced by the SR converter output transformer and 2.) the high frequency characteristics of a MOSFET version of the circuit. Both of these problems have been modelled analytically and studied experimentally with breadboard circuits.

One conclusion drawn from this work was that the high frequency operating problems deserve a great deal of further attention. In particular, more work needs to be done in the area of inductor and transformer design in the 100-300 kHz. range. Future efforts in this area should aim at providing more guidance in modelling the behavior and loss characteristics of these magnetic components. The relatively low efficiencies of these circuits above 200 kHz. may prevent application at these higher frequencies, but it also may be possible to reduce these losses somewhat with improved design techniques.

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